Service Manual

Level Generator

PS-19

Frequency range: coaxial; 80 Hz to 25 MHz
balanced; 80 Hz to 14 MHz

BN 0870/00.83

LEVEL GENERATOR PS-19

Frequency range: coaxial: 80 Hz to 25 MHz
balanced: 80 Hz to 14 MHz

Service Manual BN 870; series A...

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PREFACE, TEST EQUIPMENTS

PREFACE

INTRODUCTION TO THE SERVICE CONCEPT

Maintenance and repair are the two main tasks which occur during servicing of a piece of test equipment. The measuring set handbook, with its operating instructions, service instructions and appendix, provides all necessary information.

The operating instructions provide all necessary basic knowledge of the measuring set. Section 6 of these instructions describes all non-electrical maintenance work, such as cleaning and lubrication of moving parts, wherever such work is necessary.

The service instructions provide all special information for repair. Section 8 "checking important technical data" is used for both maintenance and repair.

The information was selected such that an experienced technician can execute all normal repair work. Tasks which generally only occur during manufacture of a measuring set have not been included.

The appendix contains all block diagrams, circuit diagrams, parts lists, and component location diagrams of the boards. In addition, it provides the necessary information for reading the circuit diagrams and for ordering spare parts. It contains a German/English/French translation list for important terms used in the appendix.

TEST EQUIPMENTS

The following list shows all recommended test equipment required for testing the measuring sets. However, equivalent test equipment made by other manufacturers may be used instead.

Recommended test equipment:

Measuring sets	Requirements	Recommended type	Manufac-turer	Use: see Section
Level generator	10 kHz to 10 MHz	PS-19/BN 870/xx	W & G	8.6.2, 7.7.2
Selective level meter	200 Hz to 180 kHz	SPM-11/BN 604	W & G	8.7.1
Selective level meter	25 MHz to 75 MHz	SPM-14/BN 830/0	W & G	8.7.3
Selective level meter	10 kHz to 25 MHz	SPM-19/BN 829/xx	W & G	8.4, 8.6, 8.7.2, 8.8, 7.7.6, 7.7.9
Calibrated level meter with accessories	80 Hz to 25 MHz	EPM-1/BN 564/0	W & G	7.7.4, 7.7.5, 8.3, 8.5
Test probe, 75 Ω		TK-10/BN 572/0	W & G	
Test probe		TKS-10/BN 668	W & G	
Test probe adaptor		TKSA-124/BN 668/00.14	W & G	
Test probe adaptor		TKSA-150/BN 668/00.11	W & G	
Test probe adaptor		TKSA-600/BN 668/00.14	W & G	
Calibration adaptor		TKSE-124/BN 668/00.24	W & G	
Calibration adaptor		TKSE-150/BN 668/00.21	W & G	
Calibration adaptor		TKSE-600/BN 668/00.22	W & G	
Universal counter	25 MHz	PM 6614/05	Philips	8.2, 7.7.2
Digital voltmeter	4 1/2 digits	8600 A	Fluke	7.6.6, 7.7.7, 7.7.8, 8.4
Calibrated attenuator	75 Ω, 0 to 60 dB	D 2053	Siemens	8.4
Return loss measuring attachment	124/150/600 Ω, 20 kHz to 1 MHz	RFZ-12 BN 810/01.00	W & G	8.6.2
Reflection coefficient measuring bridge	75 Ω, 5 MHz	RFZ-14 BN 830/00.01	W & G	8.6.1
Oscilloscope	$f \geq 150$ MHz	475	Tektronix	7.6.8, 7.7.2
RF Voltmeter	$f \geq 1$MHz, 10 MΩ/25 pF	400 E	hp	7.6.7
Logic tester	TTL, CMOS	TKL-515	W & G	7.6.9
DC power supply	0...5 V, $R_i < 200$ Ω	6960 A	hp	7.6.14

Other testing aids and special tools:

Designation	Type	Manufac turer	Use: see section
Attenuator, 40 dB	DG-940/BN 920/43	W & G	8.7.3
Terminating resistor, 75 Ω, coax.			8.7.1
Terminating resistor, 124 Ω, balanced			8.7.1
Terminating resistor, 150 Ω, balanced			8.7.1

INTRODUCTION TO THE SERVICE CONCEPT IN THE DIGITAL SECTION

The measuring set software contains several test programs. Together with other testing aids within the PS-19, it is thus possible to check the complete digital section of the PS-19 without device specific aids and, if applicable, to localize the fault*).

Troubleshooting during normal operation of microprocessor controls is generally not advisable.

Test equipment for servicing the digital section

- Signature analyser 5004 A hp
- Oscilloscope $F_{lim} \geq$ MHz
- Ohm meter (e.g. TRI-OHM, Gossen)

INTRODUCTION TO THE SERVICE CONCEPT OF THE IEC BUS BOARD, BN 853

A prerequisite for testing of the <IEC 625> interface board is that the digital functions of the measuring set with respect to the program execution and control of the device interface to the <IEC 625> interface board are functioning correctly.

All functions of the <IEC 625> interface board can then be checked by means of a go/no go test during which the measuring set is addressed via the <IEC 625> bus by an HP 85 desk computer (= <IEC 625> controller).

In the case of a fault, the <IEC 625> interface board must be replaced.

Testing aids for the IEC bus board

Measuring sets	Requirements	Recommended type	Manufacturer	Use: see section
Desk computer HP 85	Only the	HP 85	hp	7.5.2, 7.5.5
HP-IB interface for desk computer HP 85	recommended	82 937 A	hp	7.5.2, 7.5.5
ROM drawer for desk computer HP 85	types	82 936 A	hp	7.5.2, 7.5.5
Input/output ROM for desk computer HP 85	may be	0085 15003	hp	7.5.2, 7.5.5
Test program IEC Bu 1		Testing aid 2-853	W & G	7.5.2, 7.5.5
IEC-IEEE adaptor	used	S 834	W & G	7.5.2, 7.5.5

TROUBLESHOOTING IN THE AGC AMPLIFIER

The aim of the troubleshooting strategy shown in Section 7.6.14 is to detect and localize defects in the AGC amplifier and to decide whether the complete AGC amplifier must be replaced or whether a repair is possible.

Notes are provided on possible repairs, of which there are two categories: repairs where replacement of components presents no problems and repairs which require subsequent recalibration of the measuring set, which is possible only in the factory.

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*) Note:
The signatures required for testing are shown in the service instructions only if they are needed for localizing a fault to a specific board.

7 TROUBLESHOOTING AND REPAIR INFORMATION

7.1 SAFETY MEASURES

7.1.1 PROTECTION AGAINST ELECTRICAL ACCIDENTS

Satety class

This measuring set is protected in accordance with safety class I of VDE 0411 and IEC Publ. 348. The mains cable supplied with the measuring set contains a protective conductor. The mains plug may be inserted only in outlets with protective conductor connections, except in specially certified rooms. It is not permitted to disconnect the protective conductor either inside or outside the measuring set.

Opening the measuring set

If covers or parts of the measuring set are removed with tools, components carrying dangerous voltages may be exposed. Connection points may also carry dangerous voltages.

Before opening the measuring set, it must be disconnected from all voltage sources.

If calibration, maintenance, or repair is then absolutely necessary with the measuring set open and connected to the voltage supply, then this may be carried out only by a specially trained person who is familiar with the dangers to be expected.

Capacitors within the measuring set may still carry a charge after the measuring set has been disconnected from all voltage sources; see the appropriate notes in the circuit diagrams.

Fuses

Only fuses of the prescribed size and rating may be used.

Repair, replacement of parts

Repairs are to be carried out in a workmanlike manner. In particular, care must be taken that the design features of the measuring set are not modified such that the safety of the measuring set is decreased. The leakage and air gaps between components and the spacing provided by insulation must not be reduced.

Use only original parts for replacement. Other spare parts may be used only if they have no negative effect on the safety-oriented characteristics of the measuring set.

Testing after repair and maintenance

- Checking the protective conductor

Correct connection and good condition of this conductor are checked by visual inspection and by measuring set the resistance between the protective conductor pin of the plug and the chassis of the measuring set. This resistance should be $< 0.5\ \Omega$. During the measurement, the cable should be moved; any variations in the resistance indicate damage to the protective conductor.

Checking the insulation resistance.

The insulation resistance is measured with 500 V DC between the voltage pins and the protective conductor pin of the mains plug. The mains switch of the measuring set should be in the "on" position during this test. The insulation resistance should be $> 2\ M\Omega$.

7.1.2 NOTES FOR PROTECTION OF THE CIRCUIT

Caution when handling MOS components!

Some of the components used in this measuring set are MOS (metal-oxide-silicon) components. These are easily destroyed by static charges, ripple voltages from incorrectly grounded equipment, or other interference potentials. Destruction by static charges can be avoided by complying with the following rules:

- MOS components should be left in the manufacturer's packing materials until they are required for use. All pins must be connected together conductively until the component is required (black, electrically conductive foam material).
- Before removing the MOS components or printed circuit boards on which MOS components are mounted, the electrically conductive part of the packing material must be brought into contact with a conductive bench top or the chassis of the measuring set to be repaired, either of which is the reference potential.
- Before touching MOS components, grasp a conductor which acts as a reference potential with one hand.
- All tools and equipment, the circuit being repaired, and the person carrying out the repair should have the same potential as the conductor which acts as a reference potential (e.g. a conductive bench top or, alternatively, the chassis of the measuring set being repaired). For this reason, tools should be brought into contact with the reference potential before touching MOS components. Tools must not have insulated handles.
- If a printed circuit board or some other part of a measuring set is handled separately from the main measuring set, and is not laid on a conductive bench top, then the ground of the printed circuit board must be connected to the reference potential.

Destruction due to ripple voltages during soldering can be avoided by establishing a permanent connection between the soldering iron and the chassis of the measuring set being repaired.

MOS components can be identified by the letters MOS, CMOS, or MOSFET in the component designation in the spare parts list.

7.2 SOLDERING INSTRUCTIONS

The use of thin solder with a small amount of flux is recommended. The following should be noted:

- Soldering time for all components $\leq$ 5 s;
- Soldering temperatures $\leq 260^{\circ}$ C;
- Avoid splashing flux on switch contacts;
- when soldering on switch contacts or other electro-mechanical components, ensure that flux cannot creep onto the contact surface.

Instructions for removal of components with multiple pin connections:

The best method is to remove the solder from each separate pin with the aid of a special solder removal tool. After removal of solder, move the component from side to side and check that all pins are free. Do not use force: Through-plated holes are particularly sensitive to tension during soldering. In the case of dual in-line components, damage to the printed circuit board can be avoided by cutting off the pins with a high speed cutting disc on the component side and then removing each pin separately with a soldering iron.

Soldering on thin film circuits

Soldering on thin film circuits requires precise temperature control, minimum soldering time, and special soldering aids. The risk of destroying the circuit if normal soldering methods are used is so high that we recommend that the complete thin film circuit be replaced.

7.3 EQUIPMENT IDENTIFICATION

For enquiries, when ordering spare parts, or to check whether the service instructions belong to the measuring set to be repaired, the following equipment identification is required:

Type designation, designation of the special version, installed options, serial index, and serial number.

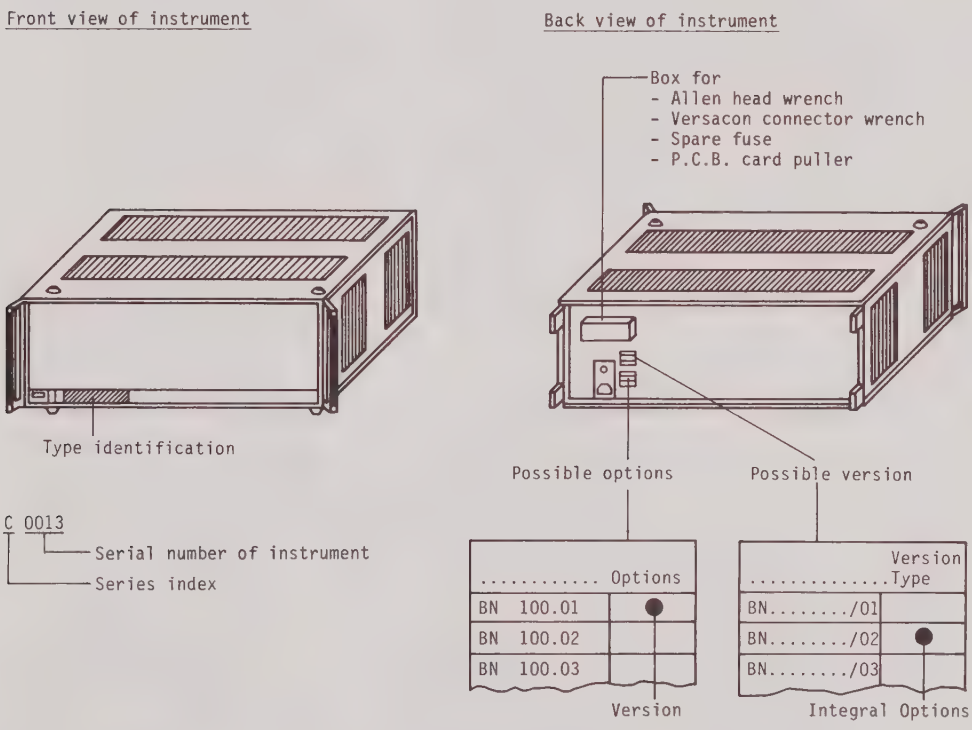


Figure 7-1 shows where the various markings are located.

7.4 STRIPPING THE MEASURING SET

See Figure 7-2 for removal of the measuring set

See Figure 7-3 for removal of knobs

See Figure 7-4 for screening trays and frames

After removal of the 6 upper Allen head screws, the instrument is lifted upwards and out from the enclosure. The power supply remains in the enclosure. It is, however, connected to the instrument by a wiring harness.

Tool:
Allen wrench, Sw = 3
(see back panel)

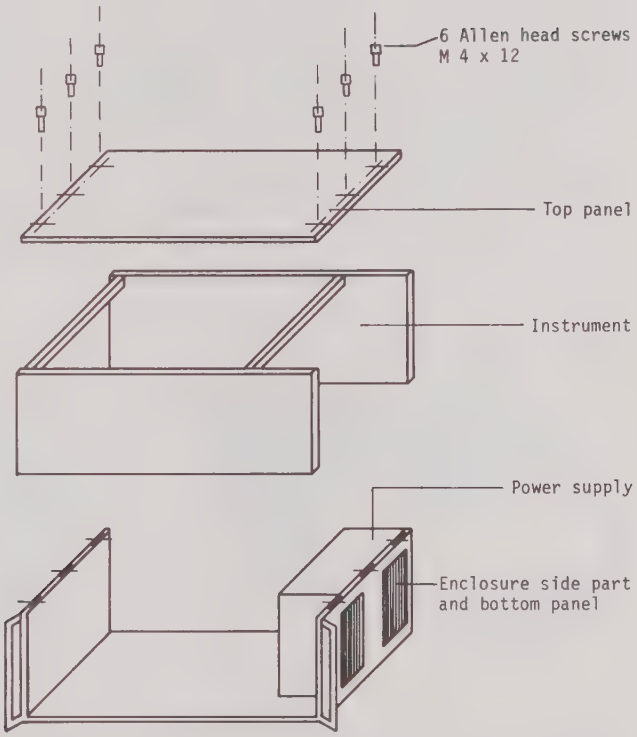
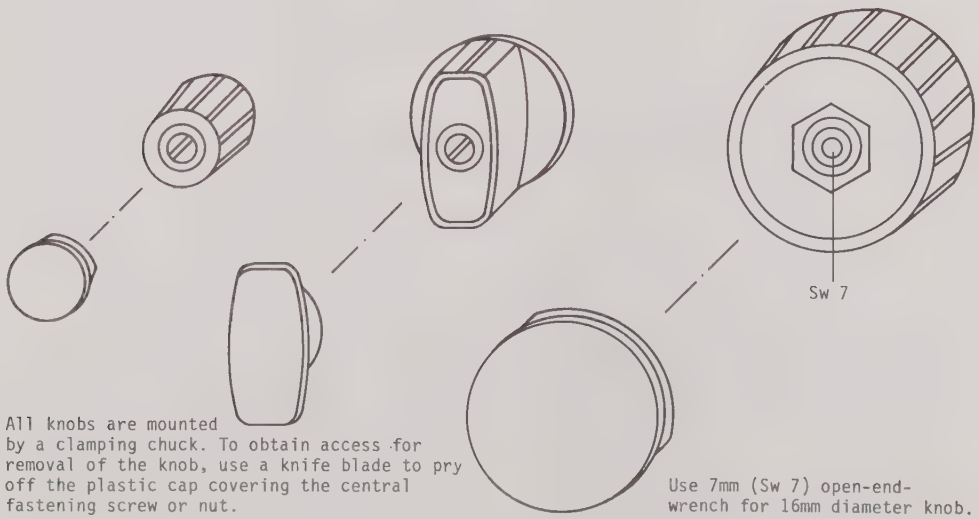


Figure 7-2 Disassembly of measuring set



All knobs are mounted by a clamping chuck. To obtain access for removal of the knob, use a knife blade to pry off the plastic cap covering the central fastening screw or nut.

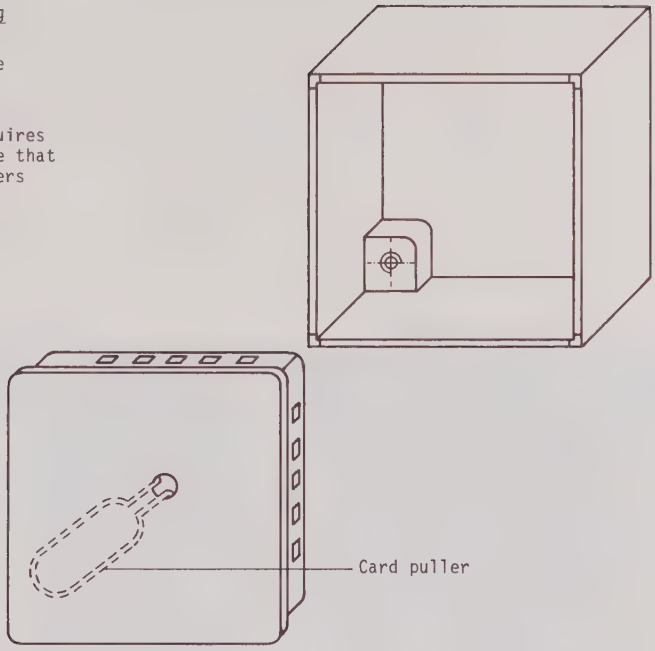
Use 7mm (Sw 7) open-end-wrench for 16mm diameter knob.

Figure 7-3 Removal of knobs

Removal of cover from screening boxes and frames

The card puller is used to take the covers off from the frames and boxes.

Caution: replacing a cover requires attention to make sure that the thin contact fingers are not damaged.



Disassembly of circuits from screening boxes and frames

The stand-off screws or spacers to which the printed circuit board is attached, and all chassis-ground screws should be removed. Then the printed circuit board is removed by the card puller.When replacing the circuit the contact pins must be protected by assuring the p.c.b. is exactly parallel to all pins before the p.c.b. is pressed home.

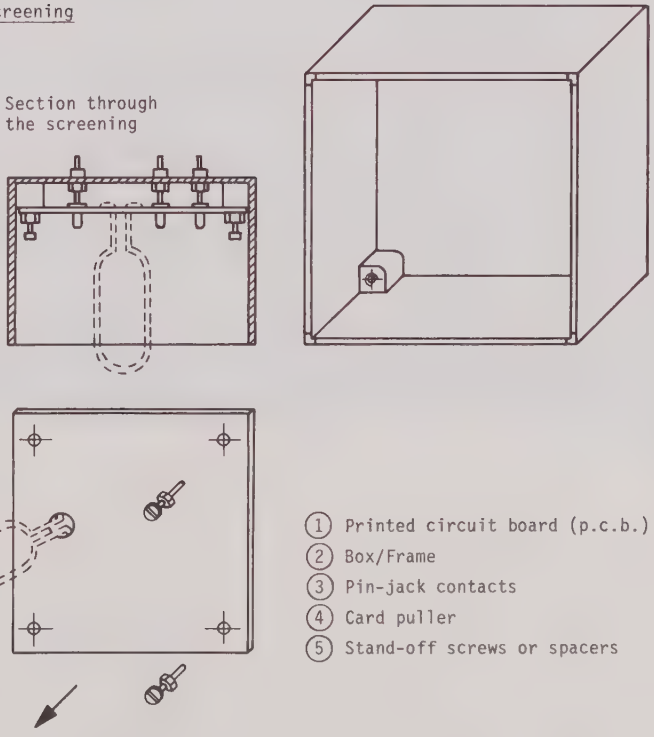


Figure 7-4 Screening boxes and frames

7.5 POSITION OF BOARDS, ALIGNMENT ELEMENTS, TEST POINTS

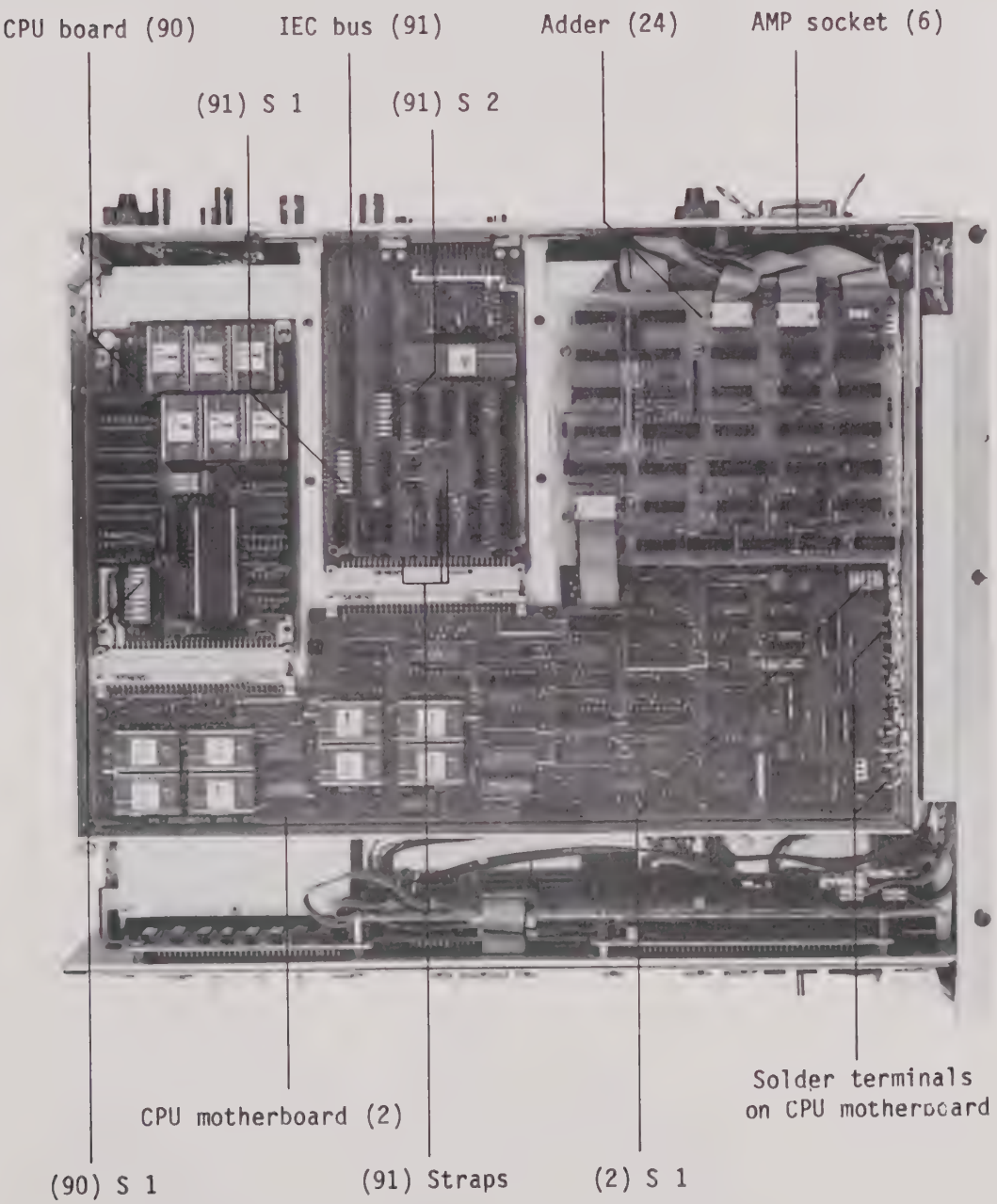


Figure 7-5 Top view of measuring instrument

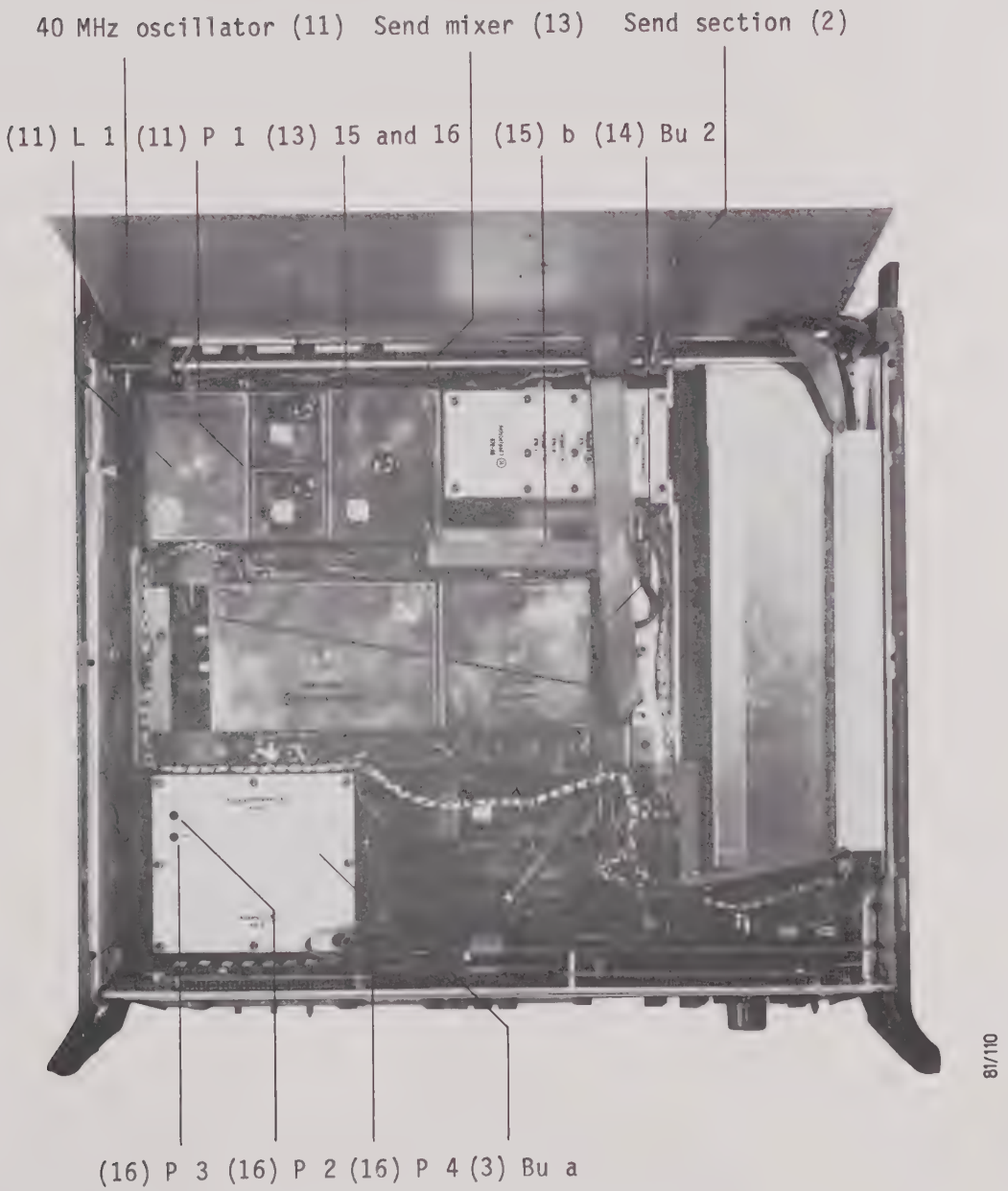


Figure 7-6 Top view of measuring instrument with control section lifted

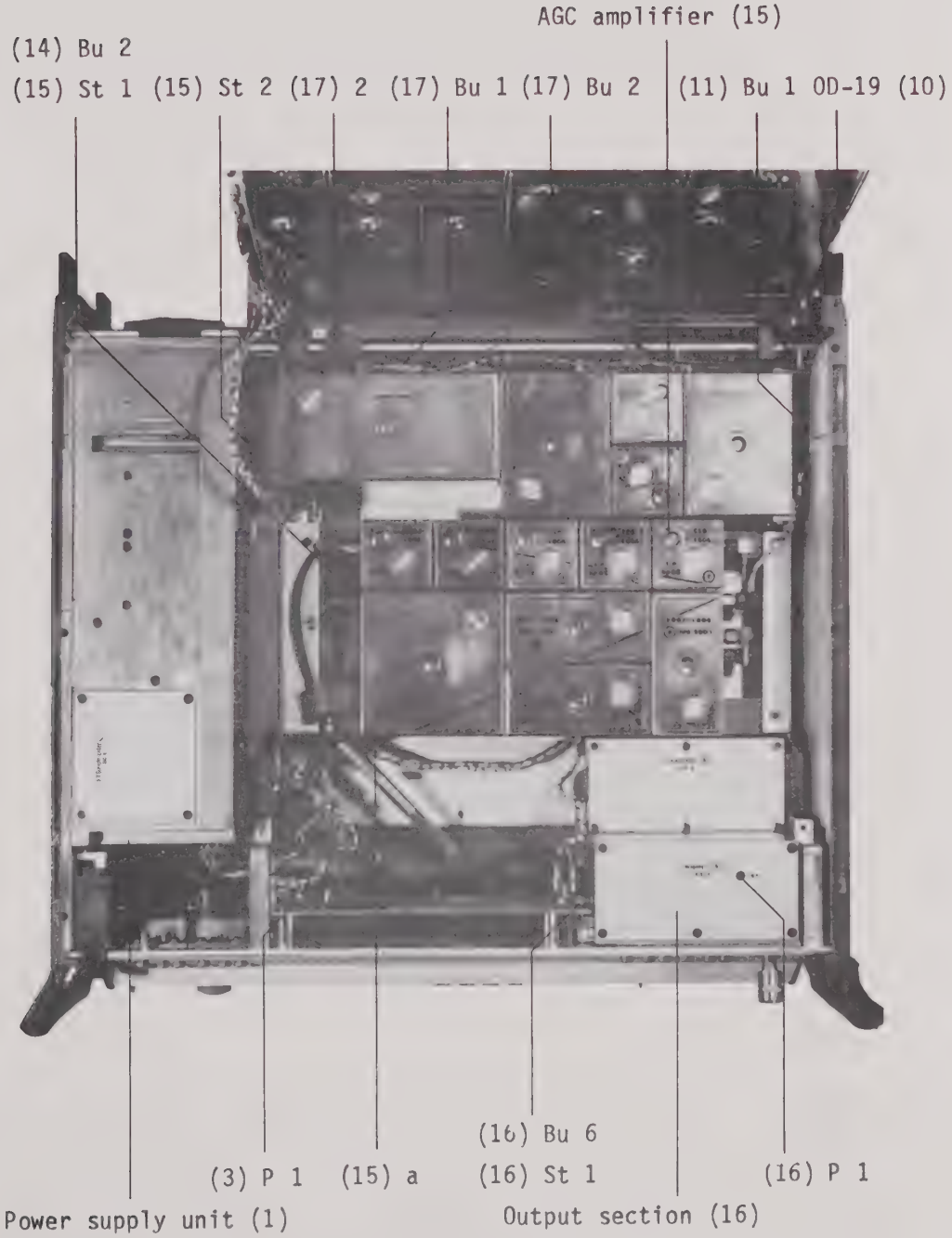


Figure 7-7 Bottom view of measuring instrument, with synthesizer lifted

7.6 TROUBLESHOOTING NOTES

7.6.1 CONCEPT OF FAULT LOCALIZATION

If the measuring set operates in an extremely abnormal manner, then the reason may be a faulty supply voltage and troubleshooting should be started with Section 7.6.7.

If the output level is incorrect (amplitude, waveform, distortion factor), then start troubleshooting with Section 7.6.7.

If meaningless front panel settings or values are displayed, or if inputs are not accepted correctly, then start with Section 7.6.2; the same applies if faults occur during use of the data interface or the IEC bus.

7.6.2 RECOMMENDED PROCEDURE FOR TROUBLESHOOTING IN THE DIGITAL SECTION

Test	Description	Notes
1.) Memory test a) Self test b) CPU and EPROM test	See service instructions Section 7.6.3.1 Section 7.6.3.3	In the case of faults, further tests are relatively useless: possibly see Section 7.6.3.3
2.) Front panel test	See service instructions Section 7.6.4	Multiple errors may also be caused by the CPU motherboard (see 3.)
3.) Test of the interfaces	See service instructions Section 7.6.5	Signature analyser and oscilloscope are required
4.) Test of the adder	See service instructions Section 7.6.6	Signature analyser and oscilloscope are required.

7.6.3 MEMORY TEST

7.6.3.1 Self test

An automatic RAM/ROM test is carried out when the PS-19 Level Generator is switched on. This test checks the read-write memory and the operating system software (ROM). The symbols 0 ... appear in the frequency display if this test has been passed. Afterwards the PS-19 resets the frequency, levels and other parameters that were previously stored.

An error number is shown in the frequency display if there is a fault in the control section.

0 ... 100 RAM fault

0 ... 200 ROM fault

7.6.3.2 Notes on signature analysis

With the aid of a signature analyzer (e.g. hp 5004A/5005A), digital signal sequences of any length can be checked uniquely and easily. Constant signatures (4-digit, pseudo-hexadecimal) are generated on the lines to be tested when defined and repeatable bit patterns exist with respect to a time window (START/STOP frame). The microprocessor is forced to generate such bit patterns by stimulus programs or external connections.

With the aid of a switch on the CPU board, the data lines ADØ ... AD7 are connected to +5 V, and line AD7 is also connected via a Schottky diode to the signal $\overline{RD}$, thus generating the "processor free-running" signal. During the read operation, data lines ADØ to AD6 are HIGH and AD7 ≅ $\overline{RD}$ = LOW. The free-running instruction is thus 7F ≅ MOV A,A. If the most significant address bit A15 is used as the time window = START/STOP frame, the processor increments through the complete address range from ØØØØ to FFFF. Each address line generates a unique signature. A signal which lies correctly within the timing condition, in the case of the µP 8085 the signal $\overline{RD}$, is used as a CLOCK signal. The time relationships between the signals CLOCK, DATA, START, and STOP must always be correct, as unstable signatures will otherwise occur. Two frequently used signatures are explained briefly below:

The signature of the Ø V line is independent of the START/STOP frame and always ØØØØ. The signature of the +5 V line is called the "CHARACTERISTIC SIGNATURE". This characteristic signature indicates whether the START/STOP frame is correctly connected and whether the edges of the START/STOP frame are correct. It also indicates that the µP is running.

If the characteristic signature occurs on an address or data line, then this indicates a short circuit to the supply voltage; if the signature ØØØØ occurs, the short circuit is to ground. If two address or data lines have the same signature, then there is probably a short circuit between these two lines.

The signatures which do not depend on the software (characteristic signature, signatures of the address lines) can be supplemented by the data line signatures. Test points next to the free-run switch on the CPU board have been provided.

By incrementing the address each memory location is addressed and read. A bit stream is produced at the test points next to the free-run switch. This bit stream contains all the data stored in the PS-19. If one selects a START/STOP frame, which, for example, contains the last possible ROM address, it is possible to check the contents of all the ROMs with eight signatures. If this check finds a fault, each ROM can be checked by altering the START/STOP frame (i.e. one could use the chip-select signals.)

7.6.3.3 Free-running signature

The main parts of the CPU board (with exception of the RAMs) can be tested with the free-running signatures.

This description assumes that the reader is familiar with troubleshooting techniques using signature analysis.

7.6.3.4 Procedure for recording signatures

With the measuring set switched off, the switches on the CPU board are set to the TEST position (S1.1 to S1.9 open, S1.10 closed). When the measuring set is now switched on, the EPROMs and the busses of the CPU board can be checked.

7.6.3.5 Measurement of data signatures and checking of EPROMs

If the signatures which are specified in the PROM-BVs for the EPROMs are correct, it can be assumed that the address bus is operating correctly but not the data bus drivers.

EPROM	IC	BV	Start/Flank	Stop/Flank	*)
ROM 0	2	XXX.9311.XXX	TP 2 ↘	TP 3 ↘	
ROM 1	3	XXX.9312.XXX	TP 2 ↗	TP 3 ↗	
ROM 2	4	XXX.9313.XXX	TP 3 ↗	TP 4 ↘	
ROM 3	5	XXX.9314.XXX	TP 4 ↘	TP 4 ↗	
ROM 4	6	XXX.9315.XXX	TP 4 ↗	TP 5 ↘	
ROM 5	7	XXX.9316.XXX	TP 5 ↘	TP 5 ↗	

Figure 7-8 Connection of the signature analyser, ground to TP 1

Clock to TP 6 ($\overline{RD}$), flank ↗.
The signature 0000 appears at Pin 18 of the EPROM being measured; the characteristic signature 7A70 appears for all other EPROMs.
The data signatures can be measured either directly on the EPROM or at one of the through-plated holes alongside S1 on the CUP board.

7.6.3.6 Measurement of address signatures

The frame is a complete cycle through all addresses.
Connection of the signature analyser:
Start and stop at TP 2, flank ↘, clock at TP 6, flank ↗, ground to TP 1
The characteristic signature is 0001.
The signatures specified here apply to the complete address bus. For this reason, the signal names rather than the IC pins are specified.

Signal	Signature
A0, SA0	UUUU
A1, SA1	5555
A2, SA1	CCCC
A3, SA3	7F7F
A4, SA4	5H21
A5, SA5	OAFA
A6, SA6	UPFH
A7, SA7	52F8
A8, SA8	HC89
A9, SA9	2H70
A10, SA10	HPPO
A11, SA11	1293
A12, SA12	HAP7
A13, SA13	3C96
A14, SA14	3827
A15, SA15	755U

Signal	Signature	
$\overline{v0}$	5FU8	
$\overline{v1}$	29A6	
$\overline{v2}$	64HP	
$\overline{v3}$	1181	
$\overline{ROM0}$	3APF	
$\overline{ROM1}$	O2H7	
$\overline{ROM2}$	2828	
$\overline{ROM3}$	5P18	
$\overline{ROM4}$	8P4P	
$\overline{ROM5}$	9840	
$\overline{ROM6}$	A277	
$\overline{ROM7}$	A68C	
$\overline{RAM0}$	3H1P	*)
$\overline{RAM1}$	9C98	*)
$\overline{RAM2}$	7649	*)
$\overline{RAM3}$	24PC	*)

*) S1.9 closed

Figure 7-9 Address signatures

*) Start $\overline{CE}$ (pin 18) of relevant PROM, neg. flank (↘), key depressed.
Stop to same pin, pos. flank (↗) (key not depressed).

EPROM/TYPE 2716

The IC is programmed with the PROM PROGRAMMER Data I/O Model 16. Before programming, the master EPROM is to be checked. The erase window of the programmed IC is to be covered with an adhesive label. See the appropriate Bv parts list for the drawing number of the adhesive label.

Bv. No.	Designation	Test code	Signatures (+ 5 V frame - 7A 70)								Series status
			D0	D1	D2	D3	D4	D5	D6	D7	
870 - 9311.005/4	90 IC 2	4E79	7876	4347	F3H9	407F	P1C2	POC6	C121	7419	A only
870 - 9311.018/4	90 IC 2	7382	HU4H	39UA	40FU	8950	52AA	2F63	45F3	PC74	B...
870 - 9312.004/4	90 IC 3	B4E4	1691	10H9	00A3	4FAU	76A5	5490	A726	36FH	A only
870 - 9312.017/4	90 IC 3	A9C5	641U	8177	8AF5	PH97	671H	325C	0555	41U4	B...
870 - 9313.003/4	90 IC 4	8613	67UC	U528	6C1P	FAFH	27U6	F473	8AU7	5AFU	A only
870 - 9313.006/4	90 IC 4	8790	3577	936P	UUF2	4C5C	F4P6	7448	727H	78PF	B...
870 - 9314.002/4	90 IC 5	5D85	C8U1	97CP	C363	IF03	8C7H	4084	FUH6	25P1	A only
870 - 9314.015/4	90 IC 5	4E3D	OCUA	FC66	H3HF	4528	694A	OUUP	C2P2	6U4F	B...

Programming instructions	Series A Bv.870-9311.005/4 and following	Sh. 1 of 3	

EPROM/TYPE 2716

The IC is programmed with the PROM PROGRAMMER Data I/O Model 16. Before programming, the master EPROM is to be checked. The erase window of the programmed IC is to be covered with an adhesive label. See the appropriate Bv parts list for the drawing number of the adhesive label.

Bv. No.	Designation	Test code	Signatures (+ 5 V frame - 7A 70) D0	D1	D2	D3	D4	D5	D6	D7	Series status
870 - 9315.001/4	90 IC 6	9332	UHP9	5C10	4HPA	U6H4	F09H	H08P	06UF	6947	A only
870 - 9315.014/4	90 IC 6	982D	5FP2	4CP6	U777	1072	1406	7A3U	A4P0	8843	B...
870 - 9316.000/4	90 IC 7	A815	7P46	F21P	5F87	408F	U7CH	1780	C330	4P2A	A only
870 - 9316.013/4	90 IC 7	B273	9F72	28PF	HA23	A60F	C6PU	9F5H	7U84	5U5A	B...
870 - 9317.009/4	2 IC 8	3D81	0446	C75P	UU99	3F69	4CC5	764H	649P	75HA	A only
870 - 9317.012/4	2 IC 8	292E	7H74	604A	CCU7	4PCH	6PH8	H03U	86P5	37AP	B...
870 - 9318.008/4	2 IC 9	D36A	2567	36C1	AFF1	8P81	48F3	PU58	978U	U3UC	A only
870 - 9318.011/4	2 IC 9	CA2A	4P18	5U19	6C21	317H	9A52	2637	H5F7	20PC	B...

Programming instructions	Series A Bv.870-9311.005/4 and following	Sh. 2 of 3	

EPROM/TYPE 2716
The IC is programmed with the PROM PROGRAMMER Data I/O Model 16. Before programming, the master EPROM is to be checked. The erase window of the programmed IC is to be covered with an adhesive label. See the appropriate Bv parts list for the drawing number of the adhesive label.

Bv. No.	Designation	Test code	Signatures (+ 5 V frame - 7A 70)								Series status
			D0	D1	D2	D3	D4	D5	D6	D7	
870 - 9319.007/4	2 IC 10	BB4D	479F	U7PH	AP57	655U	C52C	P790	9210	5A84	A only
870 - 9319.010/4	2 IC 10	B03C	10F2	5H33	UF58	495F	U12A	8469	963C	4419	B...
870 - 9320.009/4	2 IC 11	EE7F	24A3	62A1	83U2	AA52	PU74	776H	4929	43PH	A only
870 - 9320.012/4	2 IC 11	FDDB	H792	OP65	70IC	9148	6C27	H8H2	2500	AU00	B...
870 - 9321.008/4	2 IC 12	4E5C	H6U9	6UP6	75FA	9450	9PAC	H937	6CU7	8415	A only
870 - 9321.011/4	2 IC 12	070B	8217	972P	84A5	P427	H36U	74PU	FC5U	64UA	B...
870 - 9322.007/4	2 IC 13	FF40	19CP	FCC8	86F3	721H	AP12	2121	U15H	0465	A only
870 - 9322.010/4	2 IC 13	2095	6H69	86A8	7382	C221	12U1	H43A	PUA8	4F3A	B...

Programming instructions	Series A Bv.870-9311.005/4 and following	Sh. 3 of 3	

7.6.3.7 Fault procedure

If unexpected signatures are detected, or if the characteristic signature (signature of V_{CC}) is not correct, etc., check the following processor voltages:

- IC 23, Pin 6 (TRAP) < 0.8 V
- IC 23, Pin 35 (READY) must not be continuously low
- IC 23, Pin 36 (RESET IN) > 2.0 V
- IC 23, Pin 39 (HOLD) < 0.8 V

If these conditions are not maintained, the processor cannot operate correctly. The fault most probably then does not lie on the CPU board.

If the processor still does not operate as expected, the data bus signatures can be checked directly on the processor (any frame, clock, $\overline{RD}$, TP 6, flank ⎍):

ADM 0 to ADM 6	0001 (characteristic signature)
ADM 7	0000

7.6.3.8 Checking the RAM

Checking the RAM with free-running signatures is not possible. An internal test is provided in the PS-19 for checking the RAM. See service instructions Sec.7.6.3.1

7.6.3.9 Complete check

A complete check of the CPU board is not possible without special test facilities.

7.6.3.10 Switching to normal operating mode

In normal operating mode, the switches must be set as follows:

S1.1 to S1.9 closed and S1.10 open.

7.6.4 FRONT PANEL TEST

The front panel test is divided into two parts:

1.) Test of the electronic circuits for "continuous frequency input"

2.) Test of the remaining front panel elements

Part 1.)

The switches on the CPU motherboard (2) should be set as follows

S 1/1 closed
S 1/2 closed
S 1/3 open
S 1/4 closed
S 1/5 open

When the measuring set is switched on, the frequency display should indicate "P--003".

DIP Switch (S1) on the CPU motherboard

1.) Switch settings in operating condition

Normal setting

Switch	Position	Position	
S 1.1	0		Z_{out} changeover standard settings
S 1.2	0		
S 1.3	1*		Default setting
		0	Resetting of parameters valid before the mains was interrupted
S 1.4	0		Normal version
S 1.5	1		Must remain at 1 (operating condition)
S 1.6		Any	

* 1 = switch closed; 0 = switch open

2.) Switch settings while being repaired

S 1.1	S 1.2	S 1.3	S 1.4.	S 1.5	Type of test	Appears in frequency display
1	1	0	1	0	Continuous logic test	P--003
1	0	1	1	0	Front panel-stimulus	
0	1	1	1	0	CPU-stimulus	
0	1	1	0	0	IEC-stimulus	P--006
0	0	0	0	0	CPU motherboard-stimulus	P--001
1	1	1	0	0	Front panel test	P--002

The program which is now running checks the appropriate hardware and checks all states. The rotary knob remains stationary. If all parts of the circuit are operating correctly, the display "00" appears in the level display.

In the case of a fault, see the alignment measurement, Section 7.7.8.

Part 2.)

Set the switches on the CPU motherboard (2) as follows:

S 1/1 closed
S 1/2 closed
S 1/3 closed
S 1/4 open
S 1/5 open

When the unit is switched on, "P--002" appears in the frequency display.

Principle of testing pushbuttons and displays:

During the test, all pushbuttons are depressed in any sequence. Depression of the pushbutton is acknowledged by an easily remembered display. These displays are selected such that each element is tested. The display remains on as long as the appropriate pushbutton is depressed.

The following applies to all pushbuttons:

- The display "P--002" disappears or is replaced by another display as soon as depression of the pushbutton is recognized by the computer.
- All numerical displays are filled with "P" if the contact bounce suppression hardware cannot sufficiently reduce contact bounce. This display disappears after one second.
- All numerical displays are filled with "L" if an error is detected in the pushbutton matrix, for example, if a pushbutton cannot be identified uniquely by the software.

Pushbuttons beside or below an LED:

- The appropriate LED lights as long as the pushbutton is depressed.
- In the case of the pushbuttons "dBm", "dBm0", "dBr", the appropriate unit also appears in the level display.
- In the case of the pushbutton "MAN", the two LEDs are switched on alternately; the pushbutton should therefore be depressed at least twice.

Rocker switches below level display:

- The position of the depressed switch is indicated by "H" in the level display; a switch which is not depressed is indicated by "-".
- The direction of pushbutton depression is simultaneously indicated by an arrow in the level display.

Rocker switches on the bottom edge of the front panel:

- Each time the switch is depressed, the moving indicator light alongside the switch moves one step in the appropriate direction. Check both directions and all LEDs.

Digit keys:

- The appropriate digit appears on all numerical displays and the level display shows the plus symbol.

Decimal point:

- All decimal points of the LCDs which are used are switched on (2 in the level display, 9 in the frequency display).

"Minus" key:

- The minus symbol appears in the level display

Pushbutton "MHz/STO"

- "1.000.000 kHz" appears in the frequency display

Pushbutton "kHz/RCL"

- "1.000 kHz" appears in the frequency display

Pushbutton "dBm/dBm0/dBr"

- "dB" appears in the level display

Pushbutton "CLR"

- The digits 1 to 4 appears in the level display and the digits 1 to 9 in the frequency display. Check the correct sequence!

Pushbutton "STEP"

- The appropriate arrow appears in the level display.

Checking the X output Bu 23/front panel

As long as no pushbutton is depressed, a sawtooth voltage appears at the X output and should be checked with an oscilloscope.

Check for the following characteristics:

1. Voltage amplitude $\pm$ 2.5 V
2. Linearity of the decaying part of the waveform. There must be no linearity deviations (steps, etc.) visible on the oscilloscope.

Oscilloscope settings:

- Measurement of amplitude and overall linearity:
  1 V/cm, 5 ms/cm, Trigger +
- Fine measurement of linearity:
  1 V/cm, 1 ms/cm, Trigger +

It is sufficient to check the signal in the range 10 ms after the positive going edge.

7.6.5 TESTING THE INTERFACES

With the aid of the signature analyser and a sufficiently precise test, it is possible to determine whether the interfaces between the CPU motherboard and the remaining parts of the unit are operating correctly.

In order to select the stimulus program, the switches on the CPU motherboard (2) should be set as follows:

S 1/1 to S 1/5 all open.

If the unit is now switched on, the code "P--001" appears in the frequency display. If this display does not appear, due to a fault, then troubleshooting may still be possible.

The signature analyser should be connected as follows:

Start: ⌐ to TP 2*)
Stop: ⌐ to TP 5*) } on CPU board BN 879
Clock: ⌐ to TP 5*)
Ground: to TP 8*) } on CPU motherboard (2)

Short circuit R 33 on the CPU motherboard (2).

The adder p.c.b [829-B] must be removed (6 screws) if the signatures at sockets n, o, p, u, v are to be determined.

*) See appropriate board layout

After depression of the reset button on the probe of the signature analyser, the characteristic signature A680 must appear.

Now check the following signatures:

Socket h *)	
Pin 1	9250
2	21CF
3	8C89
4	8H26
5	2P07
6	4U91
7	CF9U
12	H568

Figure 7-10
Socket h signatures

Socket m *)	
Pin 1	4P90
2	3262
3	19U4
4	4393
5	4662
11	4053
12	8U43
13	0000**)
14	A680

Figure 7-11
Socket m signatures

Socket p *)	
Pin 4	9A15
5	67U4
6	31H6
8	H2CU
9	U082
10	HC93
11	129C

Figure 7-12
Socket p signatures

Socket u *)	
Pin 1	938F
2	0515
3	A680
4	CC99
7	67C4
8	AP67
9	5733
10	33HA
11	911U
12	CH4U
14	0000

Figure 7-13
Socket u signatures

If faults occur during the front panel test, the following signatures should also be checked:

Socket v *)	
Pin 3	A319
4	A434
6	A3P8
9	0538
10	FPC7
11	06AP
12	0357
14	0000

Figure 7-14
Socket v signatures

Cable harness connections *)	
No. 13	695U
14	5FF6

Figure 7-15
Cable harness signatures

Socket n *)	
Pin 1	43U1
2	819U
3	HHAU
4	5C48
5	H074
6	76U4
7	
8	0000
9	A680
10	A680
13	0000

Figure 7-16
Socket n signatures

Socket o *)	
Pin 1	AU1H
2	5525
3	41FA
4	888A
5	A24P
6	1A0A
7	54A8
8	HU94
9	A680
11	A680
12	A680

Figure 7-17
Socket o signatures

---

*) It is immaterial whether the appropriate cable is inserted or not.

**) Probe tip must blink

The following signatures should be measured at the socket of the data interface (AMP socket (6)) (no cable connected):

Pin 1	OOOO
12	OA9P
18	U4OA
19	5U6H
20	4P5H
21	H66C
22	H9UA
23	CUH9
24	5UPF

Figure 7-18 socket (6) signatures

The other pins used in this socket can only be tested if the technician has a great deal of time available.

Plug strip b

Pin 8a	26P8
8b	9O54
9a	H1H2
9b	HCO5
10a	PHFH
10b	245A
11a	6H5A
11b	2395
14b	29F3
16a	Probe blinks

Figure 7-19 plug strip b signatures

The switches on the CPU motherboard should now be moved to the following positions:
S 1/1, S 1/4, S 1/5 open, S 1/2 and S 1/3 closed.

After switch-on, the display "P--OO6" appears. After depression of the reset pushbutton on the probe, the characteristic signature 8620 appears. If the interface to the IEC bus interface and the inserted interface are both operating correctly, the signature 2CH4 must appear at pin 26b of plug strip a.

In order to avoid overloading the relays, this equipment status should be terminated as soon as possible.

7.6.6 TROUBLESHOOTING IN THE CASE OF INCORRECT FREQUENCY TUNING

If the displayed frequency and the actual output frequency are not identical, then the possible reason for the fault can be found with the troubleshooting diagram in Figure 7-20.

7.6.6.1 Checking the adder

The adder is checked with the HP signature analyser. The tables in Figures 7-22 to 7-26 contain the signatures with the corresponding details (test point, start and stop signals).

Figure 7-21 shows a sequence which can first be used to determine whether the adder is operating incorrectly. In the case of a fault, use the circuit diagram and attempt to find a group of components where the input signals have the correct signatures and the output signals have incorrect signatures. A good comprehension of the circuit is necessary for this and for further troubleshooting.

Only one test point is specified for each signature in the tables in Figures 7-22 to 7-26 (normally the output of an IC).

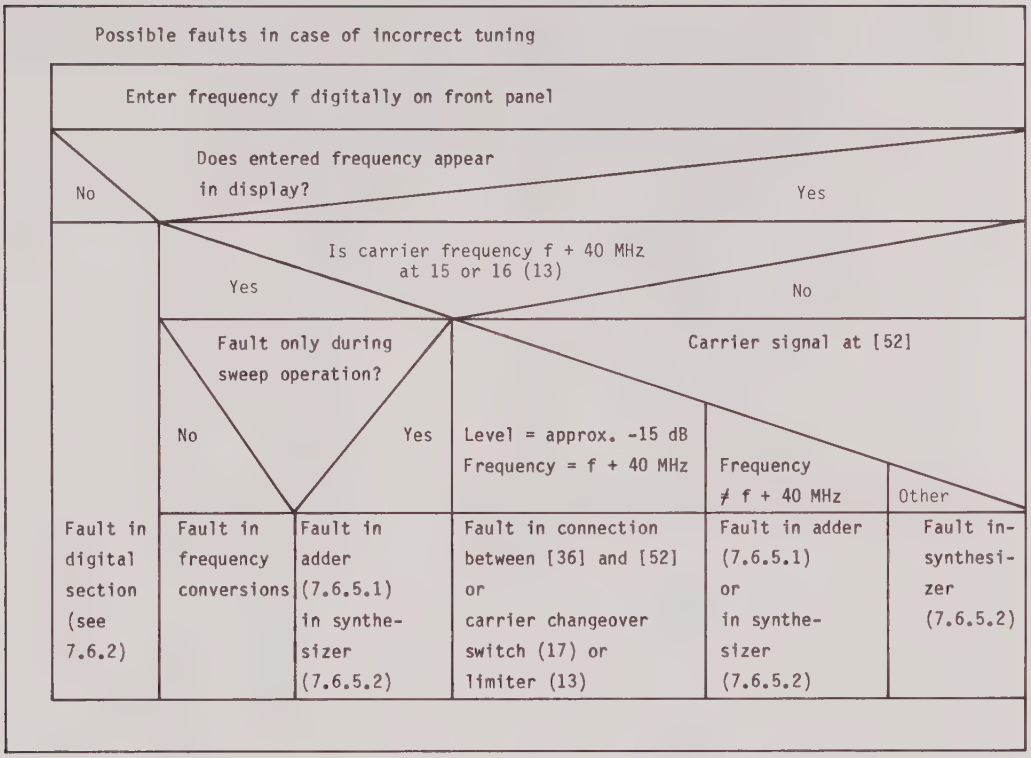

Possible faults in case of incorrect tuning
Enter frequency f digitally on front panel
Does entered frequency appear in display?
No
Yes
Is carrier frequency f + 40 MHz at 15 or 16 (13)
Yes
No
Fault only during sweep operation?
No
Yes
Carrier signal at [52]
Level = approx. -15 dB
Frequency = f + 40 MHz
Frequency ≠ f + 40 MHz
Other
Fault in digital section (see 7.6.2)
Fault in frequency conversions
Fault in adder (7.6.5.1) in synthesizer (7.6.5.2)
Fault in connection between [36] and [52] or carrier changeover switch (17) or limiter (13)
Fault in adder (7.6.5.1) or in synthesizer (7.6.5.2)
Fault in synthesizer (7.6.5.2)

Figure 7-20 Possible causes of incorrect frequency tuning

Checking the adder

Checking the shift register outputs

- Enter Δf = 26.5 MHz and switch on SWEEP/\/\[14]/RATE 0.25
- Check the signatures in accordance with Figure 7-22

Checking the control signals

- Switch off sweep operation (depress pushbutton f [8]
- Check the following signals with the oscilloscope:
  - at TP 3 and TP 4: 100 kHz
  - $\overline{DAV}$ (IC 22 Pin 8): High
  - DAC (IC 26, Pin 11): High
  - IC 26, Pin 10: High
  - IC 26, Pin 12: High
  - "Sweep on" IC 34, Pin 7: Low
- Switch on auto stop [14]
  - $\overline{DAV}$ (IC 22, Pin 8): Negative pulses of 10 to 30 µs
  - DAC (IC 26, Pin 11) Positive pulses of 10 to 30 µs
- Switch on SWEEP/\/\[14]
  - "Sweep on" IC 34, Pin 7: High

All tested signals correct?

Yes

Adder operating correctly

No

Checking the counters (IC 28 and IC 32)

- Switch on SWEEP on [14] (Δf = 26.5 MHz/RATE = 0.3 s)
- Check the signatures in accordance with Figure 7-23

Checking the digital frequency tuning

- Enter f = 12.488421 MHz and f_{STEP} = 0
- Switch on AUTO STEP [14]
- Check the signatures in accordance with Figure 7-24

Checking addition (IC 3... IC 14)

- Switch on SWEEP [14] (Δf = 26.5 MHz/RATE = 0.3 s)
- Connect IC 15, Pin 1 and IC 16, Pin 1 to "Low"
  (In series C and D measuring sets, these pins must first be disconnected from the 5 V line; in series E or later, they are decoupled via a resistor)
- Check the signatures in accordance with Figure 7-25
- Reconnect IC 15, Pin 1 and IC 16, Pin 1 to "High".

Checking the outputs of IC 15 and IC 16

- SWEEP [14] on (Δf = 26.5 MHz/RATE = 0.3 s)
- Check the signatures in accordance with Figure 7-26

Figure 7-21 Checking the adder

This signature also applies to all points which are connected to this point and should be checked at these points if an open circuit in the wiring is suspected.

Checking the shift register outputs:
Clock: ⌐ at TP 1 START: ⌐ at TP 2 STOP: ⌐ at TP 2

Test point	Signature	Test point	Signature
IC 17 Pin 5	PF5C	IC 19 Pin 5	F5P1
4	U62H	4	C545
3	UC16	3	5AA2
10	7H8C	10	AH51
13	0757	13	0964
12	03AC	12	04C2
11	81H5	11	8259
2	40PA	2	412F
IC 18 Pin 5	2P6P	IC 20 Pin 5	7951
4	9737	4	3FA8
3	FC9C	3	1P54
10	P5FH	10	0U2A
13	3385	13	7AH3
12	19F2	12	PAHF
11	0FP1	11	756P
2	0670	2	CAC7
IC 22 Pin 8	2F2A		

Figure 7-22 Checking the shift register outputs

Checking the counters:
(TP 8 = IC 31, Pin 8)
Clock: ⌐ at TP 3 START: ⌐ at TP 8 STOP: ⌐ at TP 8

Measuring point	Signature	Measuring point	Signature
IC 28 Pin 6	F9P6	IC 32 Pin 7	9515
2	P6C0	6	H082
3	2UC6	2	U6A8
12	0000	12	0000
11	70HA	11	70HA
14	70HA	14	F9P6
IC 22 Pin 8	FA84	IC 26 Pin 11	5H2U

Figure 7-23 Checking the counters

Handshake between adder and computer:
(TP 6 = IC 22, Pin 12 / TP 7 = IC 23, Pin 2)
Clock: ⌐ at TP 6 START: ⌐ at TP 7 STOP: ⌐ at TP 7

Test point	Signature
IC 26 Pin 8	0008

Data and address signals
Clock: ⌐ at TP 6 START: ⌐ at TP 7 STOP: ⌐ at TP 7

Test point	Signature	Test point	Signature
IC 1 Pin 4	0041	IC 1 Pin 5	0020
18	0009	19	0004
3	0020	2	0010
17	0010	16	0008
14	0008	15	0004
7	0040	6	0020
8	0010	9	0008
13	0020	12	0010
IC 23 Pin 11	0057	IC 23 Pin 10	002C
13	001C	12	004H
4	0062	5	0071
6	0002	7	0001

Static check of the shift registers:
Clock: ⌐ at TP 1 START: ⌐ at TP 7 STOP: ⌐ at TP 7

Test point	Signature	Test point	Signature
IC 15 Pin 7	0010	IC 16 Pin 10	0002
2	0002	15	0010
10	0008	2	0044
15	0044	7	0008
IC 17 Pin 5	0008	IC 19 Pin 5	0001
4	0004	4	0040
3	0002	3	0020
10	0001	10	0010
13	0001	13	0008
12	0040	12	0004
11	0020	11	0002
2	0010	2	0001
IC 18 Pin 5	0004	IC 20 Pin 5	0004
4	0002	4	0002
3	0001	3	0001
10	0040	10	0040
13	0022	13	0022
12	0011	12	0011
11	0048	11	0048
2	0024	2	0024

Figure 7-24 Checking digital frequency tuning

Checking the addition
Clock: ⌐ at TP 1 START: ⌐ at TP 2 STOP: ⌐ at TP 2

Test point	Signature	Test point	Signature
IC 3 Pin 5	0000	IC 4 Pin 5	0000
2	0000	2	0000
14	0000	14	0000
11	0000	11	0000
IC 5 Pin 9	922A	IC 6 Pin 9	3190
11	6ACH	11	HC36
13	5135	13	FUP3
15	IPF6	15	5U2H
10	1431	10	522H
12	APU0	12	6156
14	H143	14	C298
16	F55P	16	UH28
IC 11 Pin 13	U76H	IC 12 Pin 13	1AP7
12	AHCF	12	C6U3
11	3691	11	1A1P
10	CF91	10	HCP2
IC 15 Pin 6	3AC5	IC 16 Pin 12	5U7C
3	5FA6	13	1306
11	6UC2	4	U6F2
14	032F	5	5CU0

Figure 7-25 Checking the addition

Checking the outputs of IC 15 and IC 16
Clock: ⌐ at TP 1 START: ⌐ at TP 2 STOP: ⌐ at TP 2

Test point	Signature	Test point	Signature
IC 15 Pin 12	H8C7	IC 16 Pin 10	8CF3
7	H8C7	15	CHA3
2	A1F4	2	U5A6
10	U3C6	7	U2A3
15	670C		

Figure 7-26 Checking the outputs of IC 15 and IC 16

7.6.6.2 Checking the synthesizer

See service instructions for OD-19/BN 865, Section 7.

7.6.7 FAULTS IN THE SUPPLY VOLTAGES

Symptoms for incorrect supply voltages can be:

Front panel lamps do not light or are dim; operation of relays cannot be heard if the output sockets are switched over (switch [15]) or if the pushbutton "EXT." [7] is depressed; the synthesizer does not supply signals although the front panel controls may possibly be operated and the lamps light.

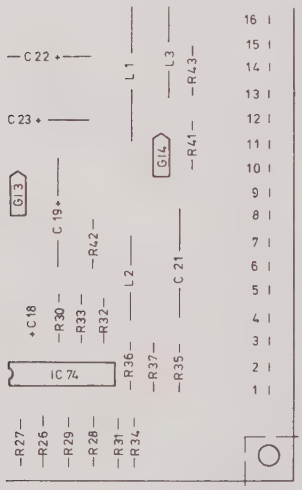
Procedure:

Mains OFF, remove case cover, lift up control section. Remove the supply voltage plugs from the output section, AGC amplifier and synthesizer.

Check the voltages on the solder terminals of the CPU motherboard; see Figure 7-27 (Caution: +6.5 V can be measured only on synthesizer plug.)

In the case of incorrect values: Unsolder the +12 V and -12 V lines from the RF chassis and again check the supply voltages.

If the supply voltages are correct:
With the measuring set switched OFF, connect the supply voltages one at a time to the output section, AGC amplifier, and synthesizer, and check after each connection.



Nominal voltages	Remarks
Approx. 0 V or +4 ... 5 V	Logic { Carrier SWITCH
Approx. 0 V or +3 ... 5 V	Logic { Signal ON
Approx. 0 V or approx. +5 V	} dB - dBm - switching
0 V	} dB - dBm - switching
0 V	
0 V	
+5 V	
-12 V	
+12 V	
+5 V (+3 ... 4 V with mains OFF)	
Approx. 0 V	Data retention

Figure 7-27 Signals on solder terminals of CPU motherboard

If the synthesizer is faulty: Check in accordance with the service instructions "OD-19/BN 865"
If the AGC amplifier is faulty: See troubleshooting strategy in Section 7.6.12.

If the measured values are still incorrect: Unsolder all lines which carry supply voltages to CPU motherboard and again check the supply voltages[1].

If CPU motherboard is faulty: Check in accordance with Section 7.6.2 "digital section"

If switching power supply unit is faulty: Check in accordance with service instructions "switching power supply unit, BN 840".

7.6.8 RF SIGNALS (LEVEL DIAGRAM) AND NOTES ON TEST POINTS

Front panel settings:
f = 20 kHz; P = 0 dBm

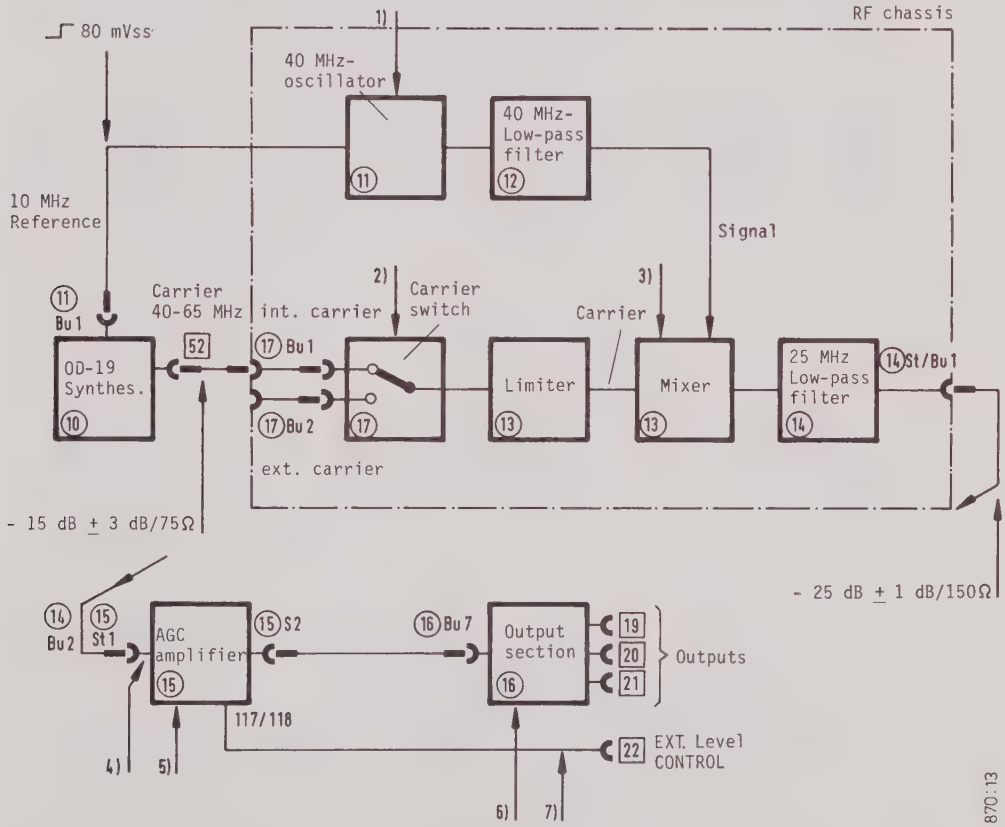


Figure 7-28 Level diagram and test points

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1) Note: In the switching power supply unit BN 840, the voltages are correct only if a specific minimum load is connected (see BN 840 Data Sheet). The voltages may differ if no load is connected.

The numbers indicate the number of the test in the table in Figure 7-27.

Levels measured with RF mV meter set to high impedance.

7.6.9 TABLE OF ADDITIONAL TEST POINTS

Front panel setting: f = 20 kHz

Test No.	Designation	Test conditions and settings	Test equipment	Test point	Nominal value/ signal shape	Probable error or further test in case of deviation
1)	Signal ON/ OFF		Voltmeter or oscilloscope	(11) 3 on [870-B] or (2) 13	+5 V: signal ON; approx. 0 V (push-button BLANK depressed): Signal OFF	Cable harness, digital section
2)	Carrier SWITCH	Carrier connection on rear of unit inserted	Voltmeter or oscilloscope > 50 MHz	(17) 2 or (2) 14	Approx. 0 V: internal carrier +5 V (pushbutton EXT. depressed): external carrier	Cable harness digital section
3)	Carrier signal	Carrier connection on rear of unit inserted	Oscilloscope > 150 MHz	(13) 15 and 16	> 800 mV_{pp}	Limiter
4)	Input level to AGC amplifier	Carrier connection on rear of unit inserted	Oscilloscope > 1 MHz	BN 9091 VARI AMP (1) 5	Sine wave 120 mV_{pp} $\pm$ 12% ($\cong$ -25 dB $\pm$ 1 dB/ 150 Ω)	Check level when terminated with 150 Ω
5)	Control of AGC amplifier	Carrier connection on rear of unit inserted	Voltmeter or oscillo-scope or logic tester	BN 9091, Sockets a and b	See tables in Figures 7-30 to 7-34	Cable or digital section
6)	Control of output section	Carrier connection on rear of unit inserted	Voltmeter or oscillo-scope or logic tester	(3) Bu a	See table in Figures 7-35 and 7-36	Cable or digital section
7)	AGC amplifier working point	Carrier connection on rear of unit inserted Level 0 dBm ↓ Level +0.1 dBm ↓ Pushbutton BLANK depressed	Voltmeter R_{in} > 1 MΩ	Bu [22] EXT. LEVEL C.	Approx. +1.1 V ... +1.5 V Increase by approx. +70 mV Further increased by approx. +40 mV	Cable from (15) 117 and 118 to Bu [22]; otherwise check the AGC amplifier in accordance with Section 7.6.12

Figure 7-29 Table of additional test points

7.6.10 CONTROL OF THE AGC AMPLIFIER BN 9091/01

7.6.10.1 Pin assignment

Socket	a	9091-7507
- 0.1 dB	1	U 705, 11
- 0.2 dB	2	U 705, 10
+ 5.2 Volt out	3	C 705; U 703-, U 704-, U 705-, 16
- 0.4 dB	4	U 705, 9
No Connection	5	No Connection
Blanking	6	U 705, 6
- 2 dB	7	U 704, 9
Corr. = 1 *)	8	U 703, 11
-20 dB *)	9	U 703, 10
- 4 dB	10	U 703, 9
- 0.8 dB	11	U 704, 11
- 1 dB	12	U 704, 10
0.01 dB Steps	13	R 615
Ground	14	Ground

*) Pos. logic.Ref. level BCD coded

a 8	a 9	
0	0	0 dB
1	0	+ 0.03 dB (Correction # 1)
0	1	-20 dB
1	1	- 0.04 dB (Correction # 2)

H	Fast
L	Slow

Figure 7-30 Pin assignments socket a

Socket	b	9091-7508
No Connection	1	No Connection
No Connection	2	No Connection
5 dB Feedback	3	U 803, 11
20 dB = 1	4	U 803, 7
No Connection	5	No Connection
10 dB	6	U 803, 5
No Connection	7	No Connection
+ 12 Volt out	8	+12 V U 801, 3..... U 802, 3.....
5 dB	9	U 803, 3
Fast / Slow **)	10	U 801, 9
20 dB # 2	11	U 803, 9
20 dB # 3	12	U 803, 14
Control Voltage Monitor	13	⑧ 94 ⟶ (⑨ 116)
Ground	14	Ground

Figure 7-31 Pin assignments socket b

TRUTH TABLE FOR R.F. ATTENUATORS								
OUTPUT LEVEL RANGE (dBm)	OUTPUT ATTN! (dB)	FEEDBACK ATTN. (dB)	PINS ON BUFFER BOARD (8)					
			b 3	b 9	b 6	b 4	b 11	b 12
			5 dB F.B.	5 dB	10 dB	20 dB #1	20 dB #2	20 dB #3
+10 ...+5.1	0	5	1	0	0	0	0	0
+ 5 ...+0.1	10	0	0	0	0	0	0	0
0 ...-4.9	5	0	0	1	0	0	0	0
- 5 ...-9.9	10	0	0	0	1	0	0	0
-10 ...-14.9	15	0	0	1	1	0	0	0
-15 ...-19.9	20	0	0	0	0	1	0	0
-20 ...-24.9	25	0	0	1	0	1	0	0
-25 ...-29.9	30	0	0	0	1	1	0	0
-30 ...-34.9	35	0	0	1	1	1	0	0
-35 ...-39.9	40	0	0	0	0	1	1	0
-40 ...-44.9	45	0	0	1	0	1	1	0
-45 ...-49.9	50	0	0	0	1	1	1	0
-50 ...-54.9	55	0	0	1	1	1	1	0
-55 ...-59.9	60	0	0	0	0	1	1	1
-60 ...-64.9	65	0	0	1	0	1	1	1
-65 ...-69.9	70	0	0	0	1	1	1	1
-70 ...-74.9	75	0	0	1	1	1	1	1

Figure 7-32 Truth table for RF attenuators

	UNBAL [19]		BAL. I [20]				BAL. II [21]							
R_i/Z	75		124		150		150/150		0/150		600/600		0/600	
Socket / Pin	a	b	a	b	a	b	a	b	a	b	a	b	a	b
1	0	NC	0	NC	1	NC	0	NC	1	NC	0	NC	0	NC
2	0	NC	1	NC	1	NC	0	NC	0	NC	0	NC	0	NC
3	+)	0	+)	0	+)	0	+)	0	+)	0	+)	1	+)	0
4	0	0	1	0	1	0	0	0	0	0	0	0	0	0
5	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	NC	0	NC	1	NC	1	NC	1	NC	0	NC	1	NC
8	0	+12V	1	+12V	1	+12V	0	+12V	0	+12V	1	+12V	1	+12V
9	0	1	0	0	1	0	0	0	0	1	0	0	0	0
10	0	X	1	X	0	X	0	X	0	X	0	X	0	X
11	0	0	0	0	0	0	0	0	1	0	0	0	0	0
12	0	0	0	0	1	0	0	0	0	0	1	0	0	0
13	X	++)	X	++)	X	++)	X	++)	X	++)	X	++)	X	++)
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 7-33 Control signals for AGC amplifier BN 9091/1, Sockets a and b (corresponding to u and v on CPU motherboard) for an output level of 0 dBm

N.C. = No connection

X = any

+) = see Figure 7-31

++) = see Figure 7-32

7.6.10.2 Control of the output section by the computer

PIN / OUTPUT / Rel.	4 / 5	10 / 4	5 / 3	9 / 2	6 / 1	8 / 6
75 Ω UNBAL	H	L	L	L	L	L
124 Ω BAL I	L	H	L	L	L	L
150 Ω BAL I	L	H	H	L	L	L
150 Ω BAL II	L	L	L	H	L	H
0 Ω BAL II	L	L	L	L	H	H
*600 Ω BAL II	L	L	L	L	L	L
0 Ω BAL II	L	L	L	L	H	L
Meaning	a	b	c	d	e	f

→ remaining pins: Figure 7-34

H = Logical high (+5 V)
L = Logical low (0 V)

* This output is active if no input signal is applied to the output section

Figure 7-34 Signals at 3 Bu a

Functions of relays 1-6

a) Relay 5 switches between BAL. and coax.
b) Relay 4 switches between BAL. II and BAL. I
c) Relay 3 switches between BAL. I 124 Ω and 150 Ω
d) Relay 2 switches between BAL. II Z = 600 Ω and 150 Ω
e) Relay 1 switches between R_{out} = Z and R_{out} = 0
f) Relay 6 switches correction value for R_{out} = 0/150 Ω BAL. II

Figure 7-35 Relay functions

Pins 1 and 14: +12 V
Pins 2 and 7: 0 V
Pins 3 and 12: -12 V
Pin 11 switches (with Relay 8) the 10 dB increased level: Increased level on: H
Increased level off: L

Checking the increased level at Pin 11:
Select output BAL. II 150 Ω/150 Ω with S [15]
Level 0.0 dBm: Pin 11 L
+10.0 dBm: Pin 11 H

Figure 7-36 Signals on 3 Bu a

7.6.11 IEC BUS board BN 853

7.6.11.1 Fitting the straps

The PS-19 uses: BN 853/05
To fit straps see Figure 7-34

Mech. documentation: see part list 853 - 8405.001
(with back panel, no coding)

El. documentation: Circuit diagram 853 - 7591.013/33

A 0	
A 128	X
B 0	
B 16	
B 32	
B 48	X
B 64	
B 80	
B 96	
B 112	
C 2	
C 4	X
C 8	
C 16	

CLR	
G	
JH	X
JL	
INTR	
R 5.5	
R 6.5	
R 7.5	X

Figure 7-37 Straps required on the IEC bus board

7.6.11.2 Board identification

An adhesive label on the IEC 625 interface board shows the series index of the interface board, e.g. A-... for Series A.

7.6.11.3 Repairing the IEC bus card

If there is a fault the IEC Bus card is replaced. It is cheaper to have the card repaired in our factory.

7.6.12 FAULTS IN THE AGC AMPLIFIER BN 9091/01

The following sections describe a procedure which first checks the correct connection condition and then tests the functions of single assemblies.

7.6.12.1 Connection conditions

- Supply voltages and their connection to the various assemblies (feedthrough capacitors);
- Control signals (see also Section 7.6.10);
- Subminax plugs, sockets, and cables at signal input and output;
- Check the input signal level terminated with the nominal value of 150 Ω:

  Rated value: -25 dB ± 1 dB to 150 Ω

  If incorrect, this level should be adjusted first (see Section 7.7.3).

7.6.12.2 Working points

Switch on the AGC amplifier and set a level of 0 dBm/75 Ω.

Measure all DC voltages specified in the circuit diagrams.
If there are any deviations in assemblies which lie within the control loop (e.g. "control loop against stop"), the best procedure is to disconnect the control loop and check it as described in Section 7.6.12.4.

7.6.12.3 Signal level

Switch on the AGC amplifier with a frequency of 20 kHz. The following table (Figure 7-35) shows the RF levels at important points in the AGC amplifier.
All measurements are carried out with a high impedance level meter and are specified in dB.

Test point	Set level in dBm	Expected value in dB	Remarks
(1) 5	0.0	-25	Input impedance and the measured value may vary due to component tolerances; permissible deviation ± 1.7 dB
(1) Q1 Base	0.0 : -4.9	approx. -33.5 : approx. -38.4	Measured value changes as set level varies from 0 to -4.9 dBm
(1) 3 (Output)	0.0 : -4.9	approx. -22.4 : approx. -27.3	Measured value changes as the level varies from 0 to -4.9 dBm
(2) Q4 emitter	0.0 : -4.9	approx. +2.2 : approx. -2.7	Measured value changes as the level varies from 0 to -4.9 dBm
(2) 14 OUTPUT A	0.0 : -4.9	-3.6 : approx. -8.5	Measured value changes as the level varies from 0 to -4.9 dBm
(2) 15 OUTPUT B	0.0 : -4.9	approx. -3.1 : approx. -8.0	Measured value changes as the level varies from 0 to -4.9 dBm
(4) 48 (= (5) R15)	0.0 : -4.9	approx. -8.1 : approx. -13	Measured value changes as the level varies from 0 to -4.9 dBm
(5) R 14	0.0 : -4.9	approx. -21.1 : approx. -26.8	Measured value changes as the level varies from 0 to -4.9 dBm
(5) 57 (= (5) R7) (= (7) 73)	0.0 · · · -4.9	approx. -8 · · · approx. -12.9	Measured value changes as the level varies from 0 to -4.9 dBm
(5) R 8	0.0 : -4.9	approx. 21.1 : approx. -26.8	Measured value changes as the level varies from 0 to -4.9 dBm
(7) U1,1	0.0	approx. -2.8	
(7) U1,7	0.0	approx. -2.8	
(7) U2,7	0.0	approx. -2.9	
(7) U2,1	0.0	approx. -2.75	
(7) TP 3		approx. -3.0	

Figure 7-38 Levels in the AGC amplifier

7.6.12.4 Open control loop

Unsolder and remove (9) R12, connect a DC power supply with $r_{out} \leq 200\ \Omega$ to solder terminal which leads to (9) C4 and (9) 114.

Set to the nominal value of +1.73 V ± 50 mV:

Assembly (1) - Vari Amp - is at its normal operating point.

With the prescribed RF input level, the levels specified in Section 7.6.12.3 should now exist.

The function of the Vari Amp can be checked by varying the DC voltage as shown in the following table.

External DC voltage ("control voltage")	Output level into 75 Ω	Remarks
Approx. ≤ +0.5 V	Approx. +5 dBm	Maximum level; "top stop"
Approx. +1 V	Approx. +4 dBm	Approx. linear range
+1.73 V	0 dBm	Working point
Approx. +2 V	Approx. -6 dBm	
Approx. ≥ +2.5 V	Approx. ≤ -16 dBm	

Figure 7-39 Characteristic cure of the Vari Amp

7.6.12.5 Possible repairs

The following list shows, for each assembly, which repairs are possible and whether realignment is necessary.

(1) VARI AMP

Components in the control path can be replaced, but not components in the RF signal path.

(2) POWER AMP

Transistors in RF path Q4, Q5 and Q6 may be replaced. If necessary, adjustment of the distortion factor should be checked.

Relays may not be replaced!

(3) WIDE BAND ATTENUATOR

Only functional checking possible; no repair

(4) LOSS SIMULATOR

Only functional check possible, including switching by the relay. The relay may not be replaced!

(5) TRACK DETECTOR

Only functional check of signal and reference paths is possible.

(6) REFERENCE GENERATOR

Repair is possible; after repair, check the absolute level of 0 dBm and the rectifier linearity as specified in Section 7.7.9 and adjust if necessary.

(7) REFERENCE ATTENUATOR
(8) RELAY BUFFER
(9) LOOP CONTROL

} Repair possible

7.7 ALIGNMENT INSTRUCTIONS

7.7.1 OVERVIEW

Trimmer	Adjustment	Section
3 P 1	Offset voltage of continuous circuit	7.7.8
11 L 1	Pulling range of 40 MHz oscillator	7.7.2
11 P 1	Oscillator level	7.7.3
16 P 1	0 dBm/124 Ω level at output BAL. I	7.7.4/8.3
16 P 2	0 dBm/150 Ω level at output BAL. II	7.7.5/8.3
16 P 3	Increased level of 10 dB at output BAL. II	7.7.6/8.4.3
16 P 4	Offset of output amplifier	7.7.7
90 S 1	Switch position on CPU board	7.6.11.7
91	Straps on IEC bus board	7.6.12
AGC amplifier assembly (15) (internal numbering as shown in circuit diagram BN 9091/1)		
(5) R 5	0 dBm/75 Ω absolute level	7.7.9
(6) R 7	0 dBm/75 Ω absolute level	7.7.9

Figure 7-40 List of all alignment elements

Assembly		Trimmer	Section
CPU motherboard (2)	Board [870-K]		
Front panel control (3)	Board [870-M]	3 P 1	7.7.8
Entry circuit (4) BN 870/01	Board [870-AB]		
Entry circuit (4) BN 870/02	Board [870-N]		
Level display (5)	Board [870-T]		
AMP socket (6)	Board [870-S]		
Carrier generator (10) OD-19 BN 865			
40 MHz oscillator (11)	Board [870-B]	11 L 1, 11 P 1	7.7.2, 7.7.3
Phase control loop (11)	Board [870-A]	11 L 1	7.7.2
Limiter (13)	Board [870-H]		
Mixer (13)	Board [870-G]	11 P 1	7.7.3
AGC amplifier (15), BN 9091/01		16 P 1, 16 P 2	7.7.4, 7.7.5
Output section (16) Output 3	Board [870-01]		

Figure 7-41 Alignment work after replacement of assemblies

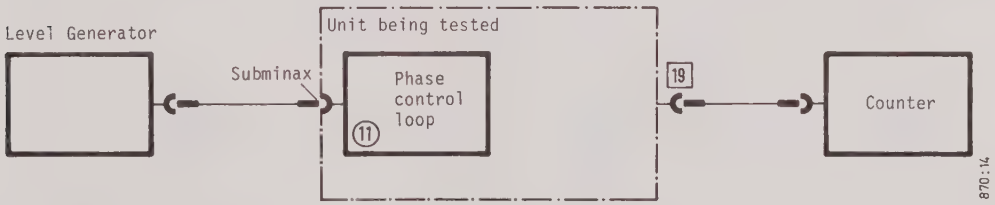
Assembly		Trimmer	Section
Output section (16) Output amplifier	Board [879-P]	16 P 4, 16 P 2,	7.7.7, 7.7.5
		16 P 3	7.7.6
Output section (16) Relay driver	Board [870-Q1]		
Output section (16) Output 2	Board [870-R]	16 P 1	7.7.4
Carrier switch (17)	Board [870-J]		
Frequency display (19)	Board [870-AA]		
Adder (24)	Board [870-B]		
CPU board (90) BN 879			7.7.9
IEC bus (91) BN 853			7.7.10
AGC amplifier (15) BN 9091/01			
(See circuit diagrams; in this assembly)			
(5) TRACKING DETECTOR		(5) R 5	7.7.9
(6) REFERENCE GENERATOR		(6) R 7	7.7.9

Figure 7-41 (continued)

7.7.2 PULLING RANGE OF 40 MHz OSCILLATOR (11 L 1)

Remove the bottom cover and swing out the synthesizer; remove the plug connector of the subminax cable (10 MHz reference frequency) from the synthesizer to the RF chassis ((11) phase control loop).

Required test equipment:
1 Level generator 10 MHz
1 Oscilloscope
1 Frequency counter



Z_{out} = 75Ω
f_{ref} = 10 MHz
Level: - 19.5 dBm/75Ω

f = 1 MHz
Level: 0 dBm/75Ω

Figure 7-42 Test configuration for pulling range of oscillator

The level generator supplies the reference frequency for the phase locked loop. If the reference frequency is varied by up to ± 300 kHz, the output frequency of the measuring set being tested must vary in the same manner.

The gate time of the counter should be set to ≤ 0.1 s.

In the case of a fault, realignment should be carried out with the aid of a test cover. If this is not available, the following alternative may be used:

Slightly adjust L1 and then close the screen cover again (!) and again check the pulling range. By a series of adjustments and measurements, it is possible to set the pulling range to a symmetrical value of at least ± 300 kHz.

7.7.3 40 MHz OSCILLATOR LEVEL (11 P 1)

Required test equipment:
1 Wide band level meter, e.g. 400 E, hp
1 Terminating resistor, 150 Ω hp

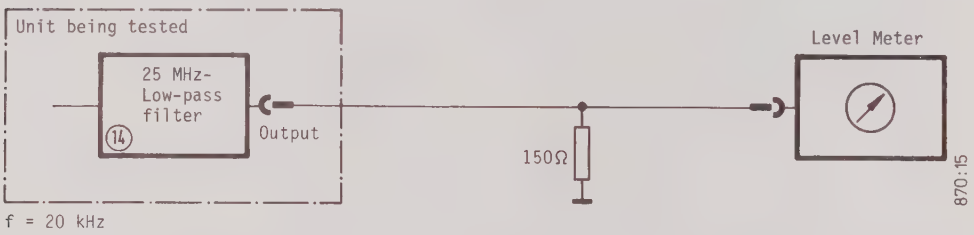


Figure 7-43 Test configuration for oscillator level

Adjust 11 P 1 for a level of -25 dB

7.7.4 0 dBm/124 Ω LEVEL AT OUTPUT BAL. I (16 P 1)

Prerequisite: A level of 0.0 dBm/75 Ω ±0.02 dB ought to be measured (with EPM-1 and TK 10) at output UNBAL [19] at f = 20 kHz and level 0.0 dBm.
Otherwise: Check/adjust as specified in Section 7.7.9

Required test equipment:
A Milliwatt Power Meter EPM-1 with TKS-10 and TKSA-124 W&G

Configuration:

Figure 7-44 Test configuration for 0 dBm/124 Ω/BAL I level

Measuring sequence:

Settings on measuring set being tested: Selected output BAL I, Z = 124 Ω, with S [15], frequency f = 200 kHz, level P_{out} = 0.0 dBm.

Adjust trimmer 16 P 1 of the output section until the level indicated on the EPM-1 is 0.00 dBm.

7.7.5 0 dBm/150 Ω LEVEL AT OUTPUT BAL. II (16 P 2)

Prerequisite: As for Section 7.7.4

Required test equipment:

1 Milliwatt Power Meter EPM-1 with TKS-10 and TKSA-150 Ω

Test configuration:

Unit being tested

Figure 7-45 Test configuration for 0 dBm/150 Ω/BAL II level

Measuring sequence:

Settings on measuring set being tested: Selected output BAL.II, Z = 150 Ω, with S [15], frequency f = 20 kHz, level is 0.0 dBm.

Adjust trimmer 16 P 2 on the output section until the level indicated on the EPM-1 is 0.00 dBm.

7.7.6 10 dB INCREASED LEVEL AT OUTPUT BAL 11 (16 P 3)

Prerequisite: 0 dBm/150 Ω level is calibrated (Section 7.7.5)

Required test equipment:

1 Level meter SPM-19 W&G

Configuration

Unit being tested

f = 20 kHz
Output BAL. II
150 Ω/150 Ω

Z_{in} = 150 Ω, balanced
0 dBm

Figure 7-46 Test configuration, increased level BAL. II

Set the measuring set to be tested to 0.0 dBm and adjust the indication on the SPM-19 to the 0 mark.

Set the SPM-19 measuring range switch to +10 dBm, set the output level on the measuring set to be tested to +10 dBm, and adjust 16 P 3 for 0 indication on the SPM-19.

7.7.7 OFFSET OF THE OUTPUT AMPLIFIER (16 P 4)

Required test equipment:

1 Digital voltmeter, resolution 0.1 mV e.g. 8600 A Fluke
1 Termination resistor 75 Ω (preferably subminax)

Configuration

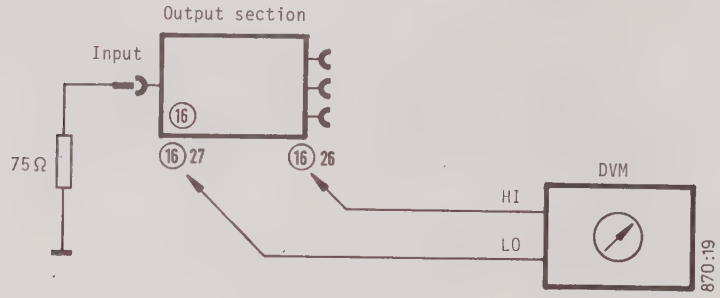


Figure 7-47 Test configuration, offset of the output amplifier

Settings: Level 0 dBm, output BAL. II, Z and R_{out} any value.

Unsolder the cable from (16) 27 and (16) 26, connect the DVM, and adjust 16 P 4 for a DC voltage of 0.0 mV

7.7.8 CONTINUOUS FREQUENCY TUNING (3 P 1)

Carry out the following adjustment on the front panel control (3):

Connect TP 2 and TP 3 together;
Adjust P 1 for a voltage of 2.5 V at TP 1.

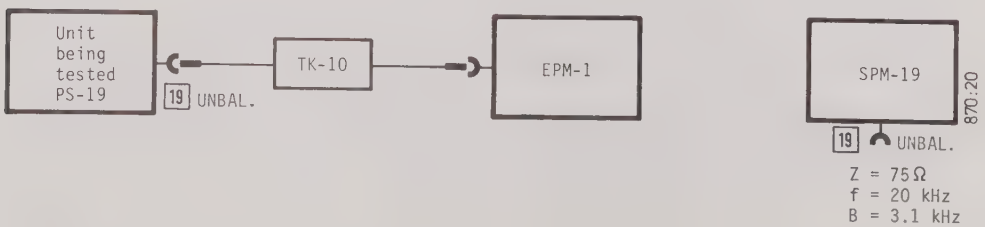
7.7.9 ABSOLUTE LEVEL 0 dBm/75 Ω

Carry out the measurements and adjustments at a temperature of $23^{o}C \pm 3$ K.

With the aid of the following two-point adjustment, the 0 dBm absolute level and the linearity of the rectifier characteristic in the tracking detector are adjusted.

Required test equipment:

1 Milliwatt Power Meter	EPM-1	BN 564/0	W&G
1 Test probe	TK-10	BN 572/0	W&G
1 Level meter	SPM-19	BN 829	W&G



Z_{out} = 75 Ω
f = 20 kHz
p = 0 dBm/75 Ω

EPM-1 calibrated
Measuring range
0 dBm +0,2 dBm

AUTO CAL: OFF
DISPLAY: ABS
SCALE: 1 dB

Figure 7-48 Test configuration

7.7.9.1 Calibration of the SPM-19

Connect the EPM-1 with probe TK-10 to Bu [19] of the measuring set to be tested, and adjust (6) R7 (AGC amplifier) for an indication of 0 on the EPM-1. If the adjustment range of the potentiometer is not sufficient, (5) R5 (AGC amplifier) may also be used. Now connect output [19] of the measuring set to be tested to input [19] of the SPM-19.

A ▌ Set the SPM-19 to the measuring range 0 dBm with the following commands:
▌ MEM 9213 RCL, 9320 RCL, 9400 RCL.

Note the value indicated on the SPM-19. This is the 0 dBm reference point for the following two-point adjustment.

7.7.9.2 Two-point adjustment

B ▌ Set the output level on the measuring set to be tested to -4.9 dBm.
▌ Set the SPM-19 to a measuring range of -4.9 dBm with the following commands:
▌ MEM 9324 RCL, 9409 RCL
▌ Adjust (5) R5 (AGC amplifier) for the same indication as at the 0 dBm reference point.

Again set up the settings in Step A - with output level 0 dBm - and adjust (6) R7 (AGC amplifier) for the same indication as at the reference point.

Carry out Steps A and B alternately until both indications are correct.

Finally, connect the measuring set to be tested and the EPM-1 as shown in the test configuration in Figure 7-48. Any remaining deviation from 0 dBm is corrected with (6) R7.

8 CHECKING IMPORTANT SPECIFICATIONS

8.1 INTRODUCTION

This section describes procedures for checking the most important characteristics of the measuring set. Wherever possible, commercially available test equipment is used.

Unless otherwise specified in the instructions, the checks should be carried out within the rated ranges of use for temperature and mains voltage.

If a warming-up period is specified in the technical data, the checks should be carried out only after this period has elapsed.

Checking of the most important data is intended to determine whether the indication of a measured parameter lies within the guaranteed error limits. Successful checking is possible without restrictions only if the intrinsic errors of the test configuration used can be neglected.

Otherwise, the following rule applies:

If the error of the test configuration used is $\pm$ m and if the guaranteed error limit for the unit to be tested is $\pm$ e, then

a value outside the limits $\pm$ (e + m)
indicates that the unit certainly lies outside the guaranteed error limits;

a value within the limits $\pm$ (e - m)
indicates that the unit certainly lies within the guaranteed error limits.

The values for e and m are specified for each measuring step. The value m depends on the test equipment used and must therefore be recalculated if equipment other than that specified is used for testing.

For systematic checking of the data, the sequence specified here should be observed. Realignment of the unit being tested should be carried out only if values outside the limits $\pm$ (e + m) are detected.

The checks in Sections 8.3 and 8.4 determine important partial errors in the output level. If the measured values lie within the partial error limits, then the overall error of the unit will also be correct.

Notes on Equipment Settings:

Unless otherwise specified for individual measurements, the following settings always apply:

PS 19:

BLANK, AUTO BLANK	[1], [10]:	OFF
Dimension	[5]:	dBm
EXT.	[7]:	OFF

SPM-19:

AUTO CAL	[1]:	ON
AFC	[5]:	OFF
MEM	[6]:	OFF
AVRG	[11]:	ON

8.2 ERROR LIMITS OF THE FREQUENCY DISPLAY

Required test equipment:

1 Universal counter	PM 6614/05	Philips

Test configuration:

Connect output [19] of the PS-19 to input A of the counter.

Equipment settings:

PS-19:

OUTPUT	[15]: Z = 75 Ω
Level	[2], [3], [4]: 0 dBm (-9 dB)
f	[8], [6], [13]: 25 MHz

PM 6614:

Frequency range	: 80 MHz (~)
Resolution	: 1 Hz

Read the frequency on the universal counter (expected value: 25 MHz).

Guaranteed error limits (e):	$\pm 3 \cdot 10^{-7} \cong \pm 7.5$ Hz
with optional accessory BN 865/00.03:	$\pm 1 \cdot 10^{-7} \cong \pm 2.5$ Hz
Error of the test configuration (m):	$= \pm 1.4$ Hz

The error of the test configuration includes aging of the universal counter over a period of one month.

8.3 ERROR LIMITS OF THE OUTPUT LEVEL AT 0 dBm

Carry out the measurement at a temperature of $23^{\circ}C \pm 3$ K.

Required test equipment:

1 Milliwatt Power Meter	EPM-1	BN 564/0	W&G
with accessories:			
1 Test probe, 75 Ω	TK-10	BN 572/0	W&G
1 Test probe	TKS-10	BN 668	W&G
1 Test probe adapter	TKSA-124	BN 668/00.14	W&G
1 Test probe adapter	TKSA-150	BN 668/00.11	W&G
1 Test probe adapter	TKSA-600	BN 668/00.12	W&G
1 Calibration adapter	TKSE-124	BN 668/00.24	W&G
1 Calibration adapter	TKSE-150	BN 668/00.21	W&G
1 Calibration adapter	TKSE-600	BN 668/00.22	W&G

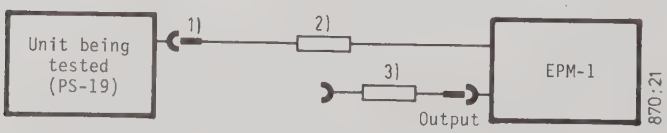


Figure 8-1 Test configuration

Note:

1), 2), 3) see Figure 8-2

Equipment settings:

PS-19:
dB/dBm changeover switch *) [31]: dBm
Level [2], [3], [4]: 0 dBm

EPM-1
Measuring range : 0 dBm ± 0.2 dBm
Calibration level switch when using TK-10 : 0 dBm, Z_{out} = 75 Ω
when using TKS-10 (Z = 124/150 Ω) : 0 dB, Z_{out} = 0
when using TKS-10 (Z = 600 Ω) : 0 dB, Z_{out} = 75 Ω

Check all three outputs of the PS-19 as follows, referring to the table in Figure 8-2:

- Calibrated of the Milliwatt Power Meter PM-1:
  Connect the test probe to the appropriate calibration adapter (see Figure 8-2) and adjust the calibration potentiometer on the meter for an indication of zero.
- Measurement:
  Connect the test probe to the appropriate output of the PS-19 and read the output level on the EPM-1.

OUTPUT (PS-19) [15]	Socket (PS-19) 1.)	Frequency (PS-19) [8],[6],[13]	Test probe (EPM-1) 2.)	Calibration adaptor (EPM-1) 3.)	Partial error limit (e)	Error of test configuration (m)
UNBAL. 75 Ω	[19]	20 kHz	TK-10		± 0.02 dB	± 0.015 dB
BAL. I 124 Ω	[20]	200 kHz	TKS-10 with TKSA-124	TKSE-124	± 0.03 dB	± 0.02 dB
BAL. I 150 Ω	[20]	↓	TKS-10 with TKSA-150	TKSE-150	± 0.06 dB	
BAL. II 150 Ω (Z_{out} = Z)	[21]	20 kHz	↓	↓	± 0.03 dB	
BAL. II 150 Ω (Z_{out} = 0)	[21]	↓	↓	↓	± 0.06 dB	
BAL. II 600 Ω (Z_{out} = Z)	[21]	↓	TKS-10 with TKSA-600	TKSE-600	± 0.09 dB	
BAL. II 600 Ω (Z_{out} = 0)	[21]	↓	↓	↓	± 0.06 dB	

Figure 8-2 Table for checking the 0 dBm level indication

Adjustment of 16 P 1, 16 P 2:

For adjustment of 16 P 1 and 16 P 2, it is assumed that the output UNBAL. 75 Ω lies within the error limits. If the output level at this output lies outside the error limits, then the output UNBAL. 75 Ω (Section 7.7.9) must be adjusted beforehand.

Warming-up period of the equipment: > 1 hour

Output BAL. I 124 Ω: Adjust 16 P 1
Output BAL. II 150 Ω (Z_{out} = Z_o): Adjust 16 P 2

In each case, adjust for an indication of 0 dBm on the calibrated EPM-1.

---

*) After operating the dB/dBm changeover switch ([31]), switch off the measuring set for a few seconds in order to activate the change.

8.4 ATTENUATION ERRORS

Required test equipment:

1 Selective level meter	SPM-19 BN 829/xx	W&G
1 Calibrated attenuator, Z = 75 Ω	D 2053	Siemens
1 Digital voltmeter	8600 A	Fluke

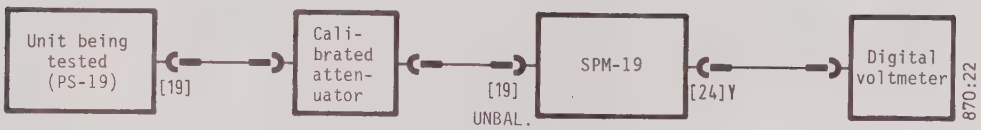


Figure 8-3 Test configuration

Equipment settings:

PS-19:

OUPUT	[15]: Z = 75 Ω
f	[8], [6], [13]: 20 kHz
Level	[2], [3], [4]: 0 dBm (-9 dB)

D2053:

Attenuation : 40 dB (≅ 41 dB with intrinsic attenuation)

SPM-19:

dB/dBm changeover switch *)	[46]: dBm
INPUT	[15]: Z = 75 Ω
DISPLAY	[3]: ABS
SCALE	[10]: 1 dB
Bandwidth	[16]: 3.1 kHz
f	[7], [12]: 20 kHz
AUTO CAL	[1]: OFF

Digital voltmeter:

Measuring range : DCV, 20 V

8.4.1 ATTENUATION ERRORS (OUTPUT AND FEEDBACK ATTN:)

These attenuators of the PS-19 are compared with the steps of the calibrated attenuator.

Vary the output level of the PS-19 and the attenuation of the calibrated attentuator as shown in the following table. At the specified attenuator positions, determine the difference between the voltage indication (DVM) and the value noted for the reference point. The sensitivity (wideband and IF gain) of the SPM-19 is not changed during the measurements. Setting at the reference points is carried out with the MEM pushbutton ([6] [12]) and a corresponding code number.

*) After operating the dB/dBm changeover switch ([31]), switch off the unit for a few seconds in order to activate the change.

Output level (PS-19) [2], [3], [4]	Calibrated attenuator/dB	Attenuator checked *)	Partial error limit (e) 1.)	Error of test configuration (m)
Set up the SMP-19 as follows: MEM 9201 RCL. 9321 RCL, 9400 RCL				
0 dBm (-9 dB)	40	Reference point	Adjust reference point to 4 V ± 20 mV 2.)	———
-10 dBm (-19 dB) -20 dBm (-29 dB) -40 dBm (-49 dB) +5 dBm (-4 dB) +10 dBm (+1 dB)	30 20 0 45 50	10 dB 20 dB No. 1 20 dB No. 1, 2 5 dB 5 dB, 5 dB (F.B.)	± 3.1 mB ≅ ± 89 mV ± 4.4 mB ≅ ± 126 mV ± 5.9 mB ≅ ± 169 mV ± 3.1 mB ≅ ± 89 mV ↓	± 2.5 mB ≅ ± 71 mV ↓
Set up the SPM-19 as follows: MEM 9202 RCL, 9331 RCL, 9400 RCL				
0 dBm (-9 dB)	60	Reference point	Adjust reference point to 4 V ± 20 mV 2.)	———
60 dBm (-69 dB)	0	20 dB No. 1 2, 3	± 5.9 mB ≅ ± 169 mV	± 3.0 mB ≅ ± 86 mV

Figure 8-4 Table for checking the attenuator error

8.4.2 ATTENUATOR ERROR (REFERENCE ATTN.)

This attenuator in the PS-19 is compared with the IF attenuator of the SPM-19.

The variable attenuator is not required for this measurement and is therefore removed from the test configuration (connect SPM-19 input directly to PS-19 output).

Vary the output level of the PS-19 and the sensitivity (WB and IF gain) of the SPM-19 as shown in the following table. At the specified attenuator settings, determine the difference between the voltage indication (DVM) and the value noted for the reference point.

The wideband and IF gains of the SPM-19 required for the measurements are entered with the MEM pushbutton and the appropriate code number.

---

*) F.B. = Feedback Attenuator
No specification = Output attenuator

1.) 0.01 dB ≅ 28.7 mV

2.) Setting the reference point:
The reference point must be set to 4 V ± 20 mV. For this purpose, the indication can be varied in steps of approximately 0.01 dB with the aid of the calibration control:
MEM 9398 RCL: Indication increases by approximately 0.01 dB
MEM 9399 RCL: Indication decreases by approximately 0.01 dB
Note the reference point for subsequent measurements.

Output level (PS-19) [2], [3], [4]	BB gain (SPM-19) /dB	MEM [6], [12]	IF gain (SPM-19) /dB	MEM [6], [12]	Stages checked	Partial error limit (e) 1.)	Error of the test configuration (m) 1.)
0 dBm (-9 dB)	-30	9213 RCL	20.0	9320 RCL 9400 RCL	Reference point	Adjust reference point to 4 V ± 20 mV 2.)	———
-0.1 dBm (9.1 dB)	↓	↓	20.1	9401 RCL	0.1 dB	±2.3 mB ≅ ±66 mV	±1.0 mB ≅ ±22 mV
-0.2 dBm (-9.2 dB)			20.2	9402 RCL	0.2 dB	↓	↓
-0.4 dBm (-9.4 dB)			20.4	9404 RCL	0.4 dB		
-0.8 dBm (-9.8 dB)			20.8	9408 RCL	0.8 dB		
0 dBm (-9 dB)	↓	↓	20.0	9320 RCL 9400 RCL	Reference point	Adjust reference point to 4 V ± 20 mV 2.)	———
-1 dBm (-10 dB)	↓	↓	21.0	9321 RCL	1 dB	±2.3 mB ≅ ±66 MV	±1.5 mB ≅ ±42 mV
-2 dBm (-11 dB)			22.0	9322 RCL	2 dB	↓	↓
-4 dBm (-13 dB)			24.0	9324 RCL	4 dB		

Figure 8-5 Table for checking the attenuator error

8.4.3 ATTENUATOR ERROR (10 dB AMPLIFIER, OUTPUT SECTION)

Required test equipment:

1 Selective level meter	SPM-19	BN 829/xx	W&G
1 Digital voltmeter	8600 A		Fluke

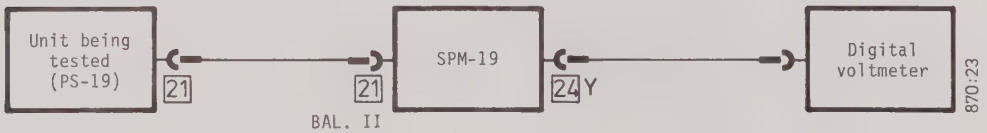


Figure 8-6 Test configuration

1), 2): See Section 8.4.1

Equipment settings:

PS-19:

OUTPUT		[15]: BAL. II, Z = 150 Ω (Z_{out} = Z)
f		[8], [6], [13]: 20 kHz
Level		[2], [3], [4] : 0 dBm (-6 dB)

SPM-19:

dB/dBM changeover switch *)		[46]: dBm
INPUT		[15]: BAL. II, Z = 150 Ω (Z_{out} = Z)
DISPLAY		[3] : ABS
SCALE		[10]: 1 dB
Bandwidth		[16]: 3.1 kHz
f		[7], [12]: 20 kHz
AUTO CAL		[1] : OFF
BB gain	MEM 9213 RCL	[6], [12]: -30 dB
IF gain	MEM 9325 RCL	[6], [12]: 25 dB

The 10 dB amplifier of the PS-19 is compared with the IF gain of the SPM-19:
- Set the reference point to 4 V $\pm$ 20 mV (see 8.4.1, 2.))
- Increase the output level of the PS-19 to + 10 dBm (+ 4 dB)
- Reduce the IF gain of the SPM-19 by 10 dB (MEM [6], [12]: 9315 RCL)

Read the deviation from the previously noted reference point on the digital voltmeter.

Partial error limit (e):	$\pm$ 1 mB $\cong$ $\pm$ 29 mV
Error of test configuration (m):	$\pm$ 2.4 mB $\cong$ $\pm$ 70 mV

Note: Checking of this error is possible only with restrictions introduced by using the specified test configuration. In the factory the unit is aligned with test equipment designed specially for the purpose.

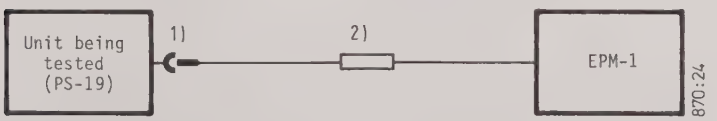
Adjustment of 16 P 3:

Adjust 16 P 3 for an indication equal to the previously noted reference point. A prerequisite for this adjustment is that the output BAL. II lies within the error limits of the output level at 0 dBm (Section 8.3).

8.5 VARIATIONS OF THE OUTPUT LEVEL WITH FREQUENCY

Test equipment:

1 Milliwatt Power Meter with accessories:	EPM-1	BN 564/0	W&G
1 Test probe, 75 Ω	TK-10	BN 572/0	W&G
1 Test probe	TKS-10	BN 668	W&G
1 Test probe adaptor	TKSA-124	BN 668/00.14	W&G
1 Test probe adaptor	TKSA-150	BN 668/00.11	W&G
1 Test probe adaptor	TKSA-600	BN 668/00.12	W&G



Note: 1), 2) see Figure 8-8

Figure 8-7 Test configuration

*) After operating the dB/dBm changeover switch ([46]), switch off the measuring for a few seconds in order to activate the change.

Equipment settings:

PS-19:

dB/dBm changeover switch *) [31]: dBm

Level [2], [3], [4]: 0 dBm

EPM-1:

Measuring range: 0 dBm ±0.2 dBm

Check all three outputs of the PS-19 as follows, using the table in Figure 8-8:

- Set the PS-19 to the reference frequency (see Figure 8-8).
- Adjust the calibration potentiometer of the EPM-1 for an indication of 0 (reference point).
- Read off the indication on the EPM-1 at the frequencies shown in Figure 8-8.

OUTPUT (PS-19) [15]	Socket (PS-19) 1.)	Probe (EPM-1) 2.)	Reference frequency/kHz (PS-19) [8] [6], [13]	Test frequencies (PS-19) [8] [6], [13]	Error limit (e) /dB	Error of test configuration (m) /dB
UNBAL. Z = 75 Ω	[19]	TK-10	20	80 Hz	±0.25	±0.01 dB
				200 Hz	±0.1	
				1; 100 kHz 5 MHz	±0.08	
				25 MHz	±0.1	
BAL. I Z = 124 Ω	[20]	TKS-10 with TKSA-124	200	60; 500 kHz 5 MHz	±0.15	±0.02/-0.03
				12 MHz	±0.2	
				14 MHz		+)
BAL. I Z = 150 Ω		TKS-10 with TKSA-150		60; 500 kHz 2 MHz	±0.25	+0.02/-0.03
				5 MHz		+)
				14 MHz	±0.2	
BAL. II Z = 150 Ω (Z_{out} = Z)	[21]		20	80 Hz	±0.25	±0.01
				200 Hz	±0.15	
				1; 100 kHz	±0.13	
				620 kHz	±0.25	
BAL II Z = 600 Ω (Z_{out} = Z)		TKS-10 with TKSA-600		80 Hz	±0.25	±0.02/-0.03
				200 Hz	±0.15	
				1; 100 kHz	±0.13	
				620 kHz	±0.25	

+) Here, there may be a slight increase in the error of the test configuration, as the errors of the EPM-1 in this frequency range are no longer guaranteed by its characteristics.

Figure 8-8 Table for checking frequency dependency of the output level.

8.6 RETURN LOSS

Note on measurement:

The return loss of the outputs UNBAL and BAL.I of the PS-19 is measured in various positions of its output attenuator, this being achieved by suitable selection of the output level. In order

*) After operating the dB/dBm changeover switch ([31]), switch off the unit for a few seconds in order to activate the change.

to avoid interference by the AGC amplifier, it is necessary to blank the output level for certain measurements. The attenuator settings remain unchanged.

The measurement is carried out at the following initial attenuator settings: 10, 15, 20, 25 dB. At output attenuator settings of < 10 dB, the AGC amplifier causes incorrect measurements. Measurements without output attenuator settings of > 25 dB do not need to be carried out, as the additional attenuators in these positions have no effect on the return loss.

The return loss of output BAL. II does not depend on the output attenuator setting (isolating amplifier!), which means that a measurement is required in only one position of the attenuator.

8.6.1 RETURN LOSS, OUTPUT UNBAL.

Required test equipment:

1 Selective level meter	SPM-19	BN 829/xx (Series D or later)	W&G
1 Return loss measuring attachment	RFZ-14	BN 830/00.01	W&G

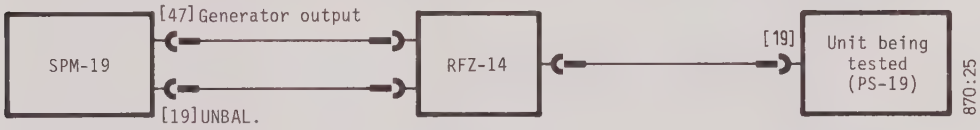


Figure 8-9 Test configuration

Equipment settings:

PS-19:

OUTPUT	[15]: Z = 75 Ω
Level	[2], [3], [4]: -5 dBm (-14 dB)
f	[8], [6], [13]: 0 MHz

SPM-19):

INPUT	[15]: Z = 75 Ω
MODE	[4]: DGTL
Bandwidth	[16]: 3.1 kHz
f	[7], [12]: 5 MHz

Calibration of the test configuration:

Do not connect the unit to be tested to the measuring attachment. On the SPM-19, depress the pushbuttons "ABS" and "REF" simultaneously. After this, depress "ABS-REF". The indication is now 0 dB (corresponding to a return loss a_r = 0 dB)

Measurement:

Connect the unit to be tested to the measuring attachment and set up the following output levels: -5 dBm (-14 dB); -10 dBm (-19 dB); -15 dBm (-24 dB); -20 dBm (-29 dB). After input of the output level, blank it (depress pushbutton "BLANK" [1]) and read off the return loss on the SPM-19.

Guaranteed error limit (e): $a_r \geq 34$ dB

Error of the test configuration (m): $m_u = 3.9$ dB

$m_l = 2.8$ dB

Example of use of the measuring error:

The guaranted error limit $a_r \geq 34$ dB is certainly
- exceeded at a measured value $a_r < 31.2$ dB $(e - m_l)$
- achieved with measured value $a_r > 37.9$ dB $(e + m_u)$

8.6.2 RETURN LOSS, OUTPUT BAL.

Some of the following specifications are enclosed within double square brackets. The specifications before the square brackets apply to output BAL. I, the specifications within the double square brackets to output BAL. II.

Required test equipment:

1 Level generator	PS-19	BN 870/xx	W&G
1 Selective level meter	SPM-19	BN 829/xx	W&G
1 Return loss measuring attachment	RFZ-12	BN 810/01	W&G

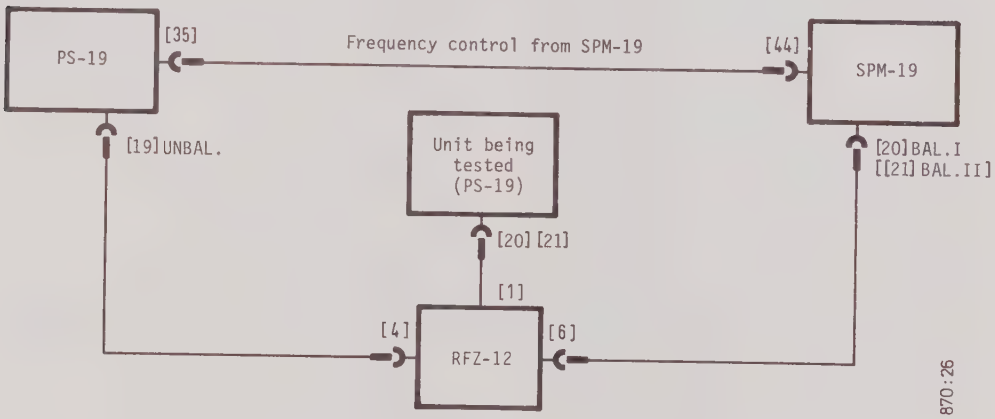


Figure 8-10 Test configuration

Equipment settings:

PS-19 (being tested):

OUTPUT	[15]: BAL. I (Z = 124 or 150 Ω)
	[[BAL. II (Z = 150 or 600 Ω)]]
Level	[2], [3], [4]: -7 dBm (-13 dB)
f	[8], [6], [13]: 0 MHz
OUTPUT	[15]: Z = 75 Ω
Level	[2], [3], [4]: +10 dBm (+1 dB)
EXT:	[7]: ON

SPM-19:

INPUT	[15]: BAL. I [BAL. II] Z = 150 Ω (Re = ∞)
MODE	[4]: DGTL
Bandwidth	[16]: 3.1 kHz

RFZ-12:

Operating mode	[7]: Balanced

Calibration of the test configuration:

Set the SPM-19 to the calibration frequency f = 60 kHz [[10 kHz]] with [7], [12]. Set switch [3] on the RFZ-12 to the required Z-value (124, 150 Ω [[150, 600 Ω]]) and disconnect the RFZ-12 from the unit to be tested (connection [1] open). On the SPM-19, depress the pushbuttons "ABS" and "REF" simultaneously. After this, depress "ABS-REF". The indication is now 0 dB (corresponding to a return loss of a_r = 0 dB).

Measurement:

Set the SPM-19 to the measuring frequency f = 1 MHz [[20 kHz]] with [7], [12] and connect the RFZ-12 to the appropriate socket of the measuring set to be tested.

On the measuring set being tested, set up the following output levels:

Output BAL. I: -7 dBm (-13 dB); -12 dBm (-18 dB); -17 dBm (-23 dB); -22 dBm (-28 dB).
Output BAL. II: Any

After input of the output level: blank the output (depress pushbutton "BLANK" [1] and read off the return loss on the SPM-19.

Output	Guaranteed error limit (e)	Error of test configuration (m)	
		m_u	m_l
Output BAL. I	$\geq$ 34 dB	2.8 dB	2.3 dB
Output BAL. II			
Z = 150 Ω	$\geq$ 34 dB	1.7 dB	1.6 dB
Z = 600 Ω	34 dB	2.8 dB	2.3 dB

Figure 8-11 Table for checking the return loss

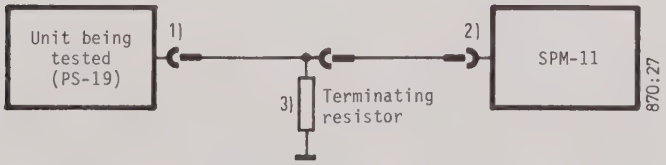
See Section 8.6.1 for example of use of the measuring error

8.7 HARMONIC DISTORTION

8.7.1 HARMONIC DISTORTION, f = 200 Hz ... 60 kHz

Required test equipment:

1 Selective level meter SPM-11 BN 604 W&G
1 Termination resistor 75 Ω, coax.
1 Termination resistor 124 Ω, balanced
1 Termination resistor 150 Ω, balanced



Note:
1), 2), 3) see Figure 8-12

Figure 8-12 Test configuration

Equipment settings:

SPM-11:

Operating mode [10]: Low distortion, slow
Bandwidth [6]: 8 Hz

Check all three outputs of the PS-19 as follows, referring to the table in Figure 8-12:

- Set up the appropriate frequency and level on the PS-19 (see Figure 8-12)
- Tune the SPM-11 to the fundamental frequency and set the indication to the reference point (0 dB) with the calibration potentiometer [5].
- After this, tune the SPM-11 to the second and third harmonics. The necessary sensitivity increase of the SPM-11 ([3]) must not exceed 60 dB.
- Read off the harmonic distortion a_{K2} and a_{K3}.

OUTPUT (PS-19) [15]	Socket (PS-19) 1.)	Frequency (PS-19) [8], [6] [13]	Level (PS-19) [2], [3], [4]	Termination resistance 3.)	Socket (SPM-11) 2.)	Measuring range for fundamental frequency (SPM-11) [3]	Error limit (e) a_{K2}, a_{K3}/dB	Error of test configuration (m)/dB
coax. Z = 75 Ω	[19]	200 Hz	+10 dBm (+1 dB)	75 Ω	[8]	0 dB	≥ 48	0.4
		800 Hz					≥ 50	0.4
BAL. I Z = 124 Ω	[20]	60 kHz	+9.6 dBm (2.7 dB)	124 Ω	[9]	0 dB	≥ 50	0.6
BAL. II Z = 150 Ω Z_{out} = 0	[21]	200 Hz	+22.9 dBm (+16.9 dB)	150 Ω	[9]	+20 dB	≥ 46	0.4
		800 Hz					≥ 50	0.4

Figure 8-13 Table for checking harmonic distortion

8.7.2 HARMONIC DISTORTION; f = 100 kHz ... 620 kHz

Required test equipment:

1 Selective level meter SPM-19 BN 829/xx W&G

Test configuration:

Connect output [21] of the PS-19 to input [20] (BAL. I) of the SPM-19.

Equipment settings:

PS-19:

OUTPUT [15]: BAL. II, Z = 150 Ω (Z_{out} = 0)
Level [2], [3], [4]: +10 dBm (+4 dB)
f [8], [6], [13]: 100 kHz or 620 kHz

SPM-19:

INPUT [15]: BAL. I, Z = 150 Ω (Z_{out} = 0)
MODE [4]: DGTL
Bandwidth [16]: 3.1 kHz
f [7], [12]: 100 kHz or 620 kHz

On the SPM-19, depress the pushbuttons "ABS" and "REF" simultaneously, then depress "ABS-REF". The indication is now 0.00 dB.
Tune the SPM-19 to the second and third harmonics of the output frequency of the PS-19 and read off the harmonic distortion a_{K2} and a_{K3}.
Increase the level of the PS-19 to +22.9 dBm (+16.9 dB) and repeat the measurements.

	f = 100 kHz	f = 620 kHz
Guaranteed error limit (e): a_{K2}, a_{K3}	$\geq$ 50 dB	$\geq$ 46 dB
Error of the test configuration (m)		
at output level +10 dBm (+4 dB):	0.6 dB	0.5 dB
at output level +22.9 dBm (+16.9 dB):	An error for the test configuration cannot be specified in this level range, as the SPM-19 is operated outside the range guaranteed by its characteristics.	

8.7.3 HARMONIC DISTORTION, f = 25 MHz

Required test equipment:

1 Selective level meter	SPM-14	BN 830/0	W&G
1 Attenuator, 40 dB	DG-940	BN 920/43	W&G

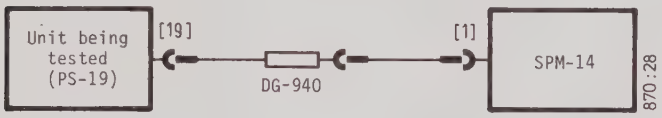


Figure 8-14 Test configuration

PS-19:

OUTPUT	[15]: Z = 75 Ω
Level	[2], [3], [4]: +10 dBm (+1 dB)
f	[8], [6], [13]: 25 MHz

SPM-14:

Operating mode	[7]: Low distortion
Bandwidth	[8]: 2.3 kHz
Scale	[6]: -90 ... 0
Measuring range	[5]: 0 dBm
f	[33], [43]: 25 MHZ

Tune the SPM-14 to the fundamental frequency (25 MHz) and adjust to the reference point (scale indication -30 dB) with the CAL potentiometer [4]. After this, tune the SPM-14 to the second harmonic (50 MHz) and the third harmonic (75 MHz) and read off the indication.

Guaranteed error limit (e):	a_{K2}, a_{K3}	$\geq$ 50 dB
corresponds to an indication on the SPM-14		$\leq$ -80 dB
Error of the test configuration (m):		3 dB

8.8 BLANKING ATTENUATION

Required test equipment:

1 Selective level meter SPM-19 BN 829/xx W&G

Test configuration:

Connect output [19] of the PS-19 to input [19] (coax.) of the SPM-19.

Equipment settings:

PS-19:

OUTPUT [15]: Z = 75 Ω
Level [2], [3], [4]: +10 dBm (+1 dB)
f [8], [6], [13]: 25 MHz

SPM-19:

INPUT [15]: Z = 75 Ω
MODE [4]: DGTL
Bandwidth [16]: 3.1 kHz
f [7], [12]: 25 MHz

Depress the pushbuttons "ABS" and "REF" on the SPM-19 simultaneously, then depress "ABS-REF". The indication is now 0.00 dB.

Blank the output signal of the PS-19 with "BLANK" ([1]) and read off the blanking attenuation on the SPM-19.

Guaranteed error limit (e): $\geq$ 80 dB
Error of the test configuration: $\pm$ 0.2 dB

9 FUNCTIONAL AND CIRCUIT DESCRIPTIONS

9.1 FUNCTIONAL DESCRIPTION OF THE COMPLETE UNIT

See block diagram 870-7500

The level generator PS-19 operates on the well-known principle of the beat frequency generator and is characterized by its wide frequency range of 80 Hz to 25 MHz unbalanced or 80 Hz to 14 MHz balanced, its frequency and level accuracy, and its ease of use. These characteristics make it particularly suitable for use in development and also for erection and monitoring of multi-channel carrier frequency systems down to the channel level. Due to the fact that all unit functions are controlled by a built-in microprocessor, which permits remote control of all of these functions via a standard data interface (IEC Bus 625), the PS-19 can be used equally well in automatic production lines or in computer-supported measuring setups. Together with the selective level meter SPM-19, it is possible to use a wide range of automatic measuring sequences, for which a special data interface is planned.
The following sections describe the most important measuring set functions with the aid of the block diagram.

The greatly simplified block diagram shows the main functional groups:

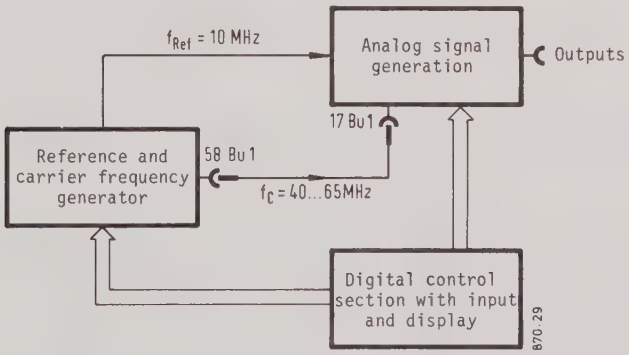


Figure 9-1 Simplified block diagram of the PS-19

The group "normal and carrier frequency generation" requires no further description in this manual, as this is in fact the synthesizer OD-19, BN 865. The only point which should be noted is that the injection of the carrier frequency from the OD-19 into the analog section of the PS-19 is carried out via a cable connection on the rear of the PS-19 (connection from 58 Bu 1 to 17 Bu 1). In contrast to this, the standard frequency is connected within the unit. This arrangement was selected for design reasons.

9.1.1 ANALOG SECTION

The analog section of the PS-19 consists of assemblies (11) to (17). Assembly (11) generates the signal frequency f_z = 40 MHz in a phase-locked loop which is locked to the standard frequency f_{ref} = 10 MHz. This value of the signal frequency, namely 40 MHz, is given by the design of the level meter SPM-19, in which the first intermediate frequency is 40 MHz. The fact that the signal frequency in a beat frequency generator coincides with the first intermediate frequency in a heterodyne receiver makes it possible to operate both units with a single tuning oscillator (e.g. for sweep operation) and thus to tune the transmitter and receiver exactly to the same frequency.

The 40 MHz signal generated (11) passes through the 40 MHz low-pass filter, assembly (12) which removes most of the harmonic frequencies. This is necessary in order to prevent the creation of certain non-harmonic spurious frequencies in the following mixing stage.

Mixing of the 40 MHz signal frequency with the carrier frequency 40 MHz...65 MHz is carried out in assembly (13), limiter and mixer. This receives the carrier frequency voltage via assembly (17), carrier switch. The carrier switch makes it possible to operate the PS-19 either with the internal carrier oscillator (OD-19) or with an external carrier frequency source. The output signal of the mixer is the difference between the carrier and signal frequencies, and is the actual generator signal in the range 0 to 25 MHz.

As the mixer, in addition to the difference signal, also generates the sum signal of both input signals, together with residual signal and carrier frequencies and multiples thereof, it is followed by a 25 MHz low-pass filter, assembly (14). This attenuates all unwanted frequencies and allows only the wanted signal to pass.

After this conditioning, the frequency of the signal is correct, but the amplitude is not yet correct for output. Firstly, its level is too low, and secondly, its level varies due to the frequency-dependent characteristics of the mixer and 25 MHz low-pass filter.

The signal is amplified to the required level in the following AGC amplifier, assembly (15), where it is also regulated to a constant amplitude by an amplitude control circuit. In addition to these characteristics, the amplifier must also provide the required generator output level.

This is done by a calibrated attenuator in the output path, which varies the level in 5 dB steps, and by a switchable voltage divider in the reference path of the AGC circuit. The adjustment range of this divider is 0 to -4.9 dB in steps of 0.1 dB. Furthermore, two fine level corrections are carried out in this reference path when various output impedances are selected with the PS-19 operating in dBm mode.

The AGC amplifier has two further tasks. If the output signal of the PS-19 is blanked or unblanked, then this operation must be carried out gradually. This "soft blanking" is carried out by the AGC amplifier when requested to do so via a control line. In addition to this, the 40 MHz oscillator (11) is switched off; this provides the necessary large blanking attenuation. The second additional task concerns the facility for external level control. For this purpose, an external amplitude control loop can be constructed, for example with an EPM-1, and with socket 15 Bu 1 as the control input via which the amplifier is controlled such that it operates as a control element for the external control loop. The output section, assembly (16), the last element of the analog signal path, finally distributes the signal coming from the AGC amplfier to the various outputs. Output UNBAL. is the direct output of the AGC amplifier (15); the outputs BAL. I and II are fed by balancing transformers. In the case of output BAL. II, a further special feature must be mentioned: The balancing transformer is preceded by an amplifier. This permits an impedance $Z_{out} \approx 0\ \Omega$ to be achieved at output BAL. II and also permits the level at this output to be increased by 10 dB.

9.1.2 DIGITAL SECTION

The lower half of the block diagram shows the digital section. This is divided into the following elements:

- CPU board
- CPU motherboard

} Central processing unit for all control tasks (BN 879)

} Extension of the CPU board (memory), together with various auxiliary circuits and interface functions, assembly (2)

- IEC Bus Interface BN 853
- Front panel group, divided into four boards, assemblies (3), (4), (5), and (19)
- Adder, intelligent interface to synthesizer, assembly (24).

9.1.2.1 CPU board

The CPU board contains, in addition to the processor, the major part of the program memory and one third of the RAM. The RAM (CMOS module) is non-volatile as it is supplied by an accumulator in the power supply unit when the measuring set is switched off, which means that the stored data remain available even with the power off.

9.1.2.2 CPU motherboard

The RAM is the same as on the CPU board (see above), but twice the size. Part of the EPROM is also used as a program memory, the rest being available for tables (fixed frequencies, etc., some of which are customer-specific).

The output ports are parallel interfaces to the output section and AGC amplifier, oscillator, and carrier switch. Via the input port, the processor can interrogate the state of switch 2S2 on the rear of the unit and of the coding switches on the CPU motherboard.

The power-on and power-off logic supplies the processor with a reset signal when power is switched on. Furthermore, the RAM is protected against uncontrolled write operations from the time when power is switched off until the power-on sequence is complete.

The voltage monitor for the accumulator determines whether the RAM supply voltage was sufficient for maintenance of data while the unit was switched off.

The data interface to the SPM-19 is the transition point to the processor bus of the SPM-19 (handshake traffic).

9.1.2.3 IEC bus interface

The interface board is plugged into a socket strip on the CPU motherboard. It is connected directly to the bus of the processor.

9.1.2.4 Front panel group

The front panel control consists mainly of auxiliary circuits for connection of displays and the entry circuit. In addition to the D/A converter for the X output, the front panel control contains a further circuit with which rotation of the tuning knob on the front panel is converted into a form which can be processed by the computer.

9.1.2.5 Adder

The adder is simultaneously the parallel interface to the synthesizer and the interpolation computer. During sweep operations, the computer program calculates only the coarse frequency steps and an increment for the fine steps. The actual fine stepping is then carried out by hardware in the adder.

9.2 CIRCUIT DESCRIPTION

9.2.1 CPU MOTHERBOARD (2)

Circuit diagram 870-7502

The CPU motherboard is divided electrically and, to a great degree, mechanically, into four sections:

- ROM area with address bus ($ROA_0 \ldots ROA_{13}$) and data bus ($ROD_0 \ldots ROD_7$).
- RAM area with address bus ($RA_0 \ldots RA_7$), write data bus ($SDB_0 \ldots SDB_7$) and read data bus($LDB_0 \ldots LDB_7$)
- The interface from the RAM area to the IEC Bus Interface, address bus and data bus ($IDB_0 \ldots IDB_7$)
- The complete I/O area from the RAM area, with the address bus $IOA_0 \ldots IOA_5$ and data bus $DB_0 \ldots DB_7$. This area has its own timing control which is independent of the processor timing.

The CPU motherboard also contains a few auxiliary circuits.

9.2.1.1 ROM area

The functions of this area differ only slightly from those of the CPU board BN 879: see the description of this board.

9.2.1.2 RAM area

In order to achieve a bus width of 8 bits, 4 bit wide RAM circuits are connected in pairs for parallel operation.

- Addressing:

  The decoders IC 21 and IC 22 generate the selection signals for the various RAM circuits from the addresses A_8 to A_{15}. The signal $\overline{V_3} = \overline{A_{14} \wedge A_{15}}$ is generated from the addresses A_{14} and A_{15} on the CPU board. The signal "$\overline{\text{CPU-RAM}}$" activates the RAM on the CPU board.

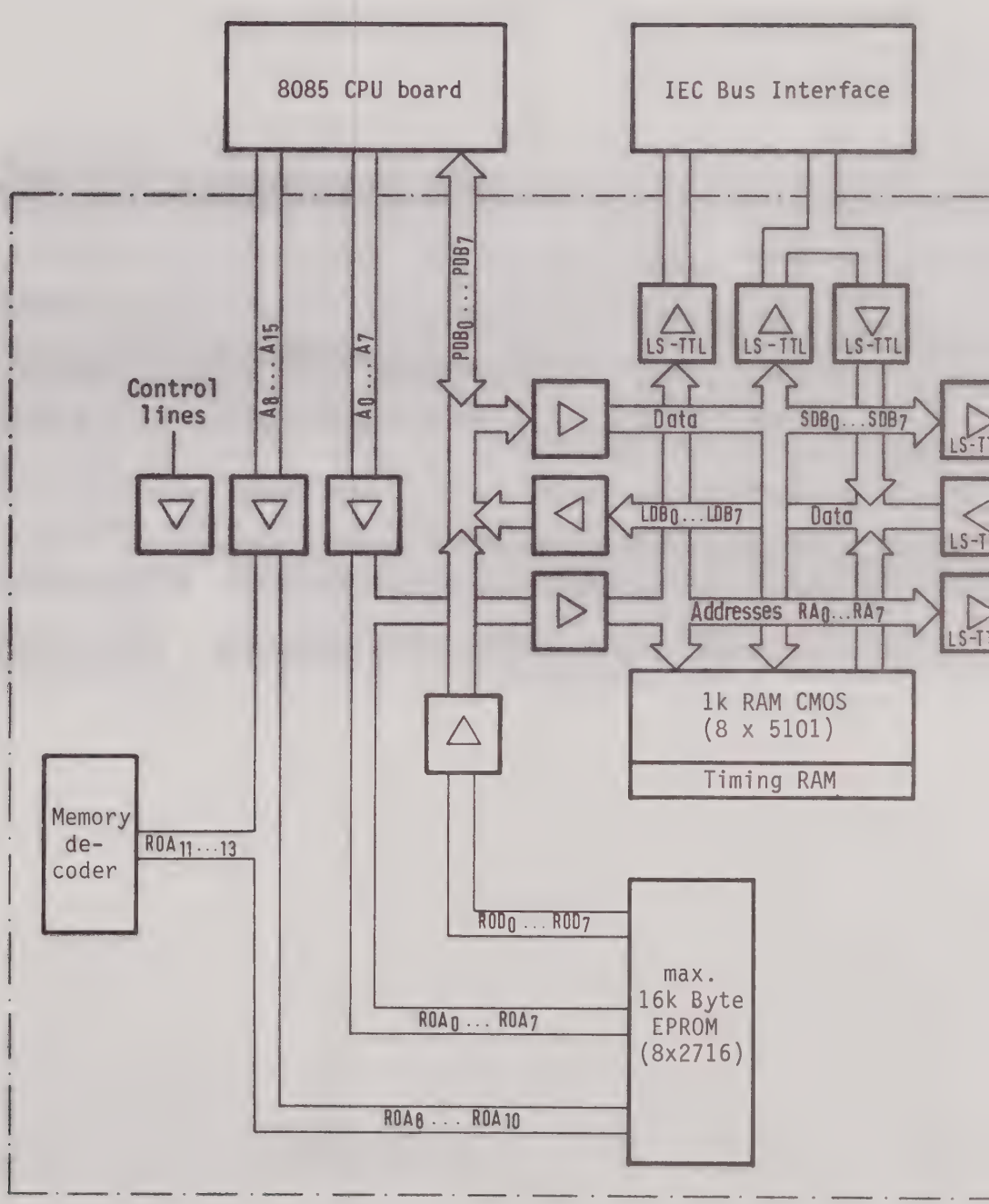
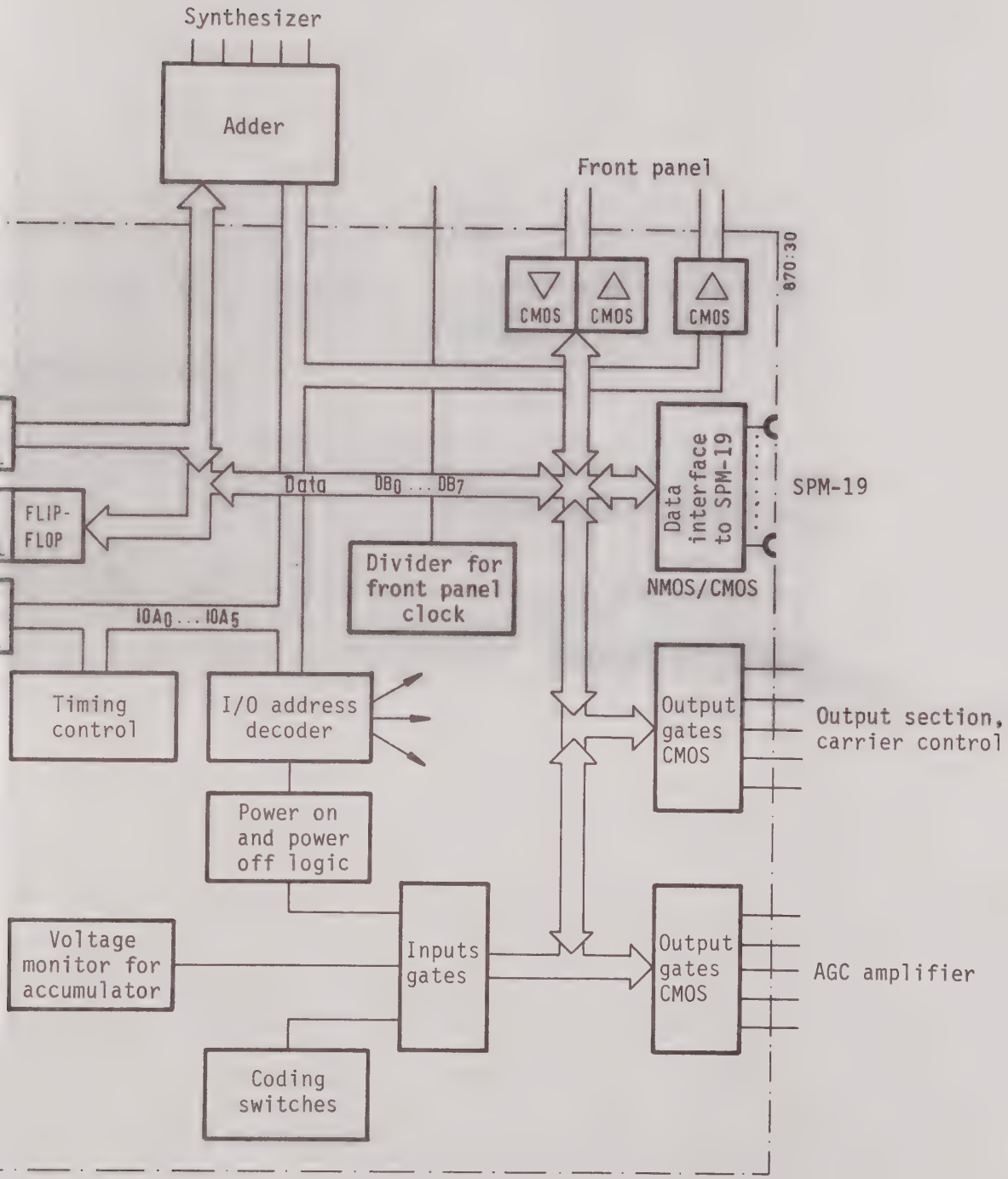


Figure 9-2 Block diagram of CPU motherboard


Synthesizer
Adder
Front panel
CMOS
CMOS
CMOS
870:30
Data
DB0 ... DB7
Data interface to SPM-19
SPM-19
NMOS/CMOS
FLIP-FLOP
Divider for front panel clock
IOA0 ... IOA5
Timing control
I/O address decoder
Output gates CMOS
Output section, carrier control
Power on and power off logic
Voltage monitor for accumulator
Inputs gates
Output gates CMOS
AGC amplifier
Coding switches

The address bits A_0 to A_7 are switched via IC 19 to the RAM only when a memory byte of the RAM (A_{15} = 1) or of the I/O area (IO/$\overline{M}$ = 1) is to be addressed (IC 7/2). This condition is stored in latch IC 24 with the ALE strobe.

- Write operation:

  If a byte in the RAM of the CPU motherboard or an output port is addressed (output IC 23/4 is then high), the driver IC 17/1 /IC 18/1 is activated with the leading edge of the WR strobe (PDB→SDB). Due to the flip-flop IC 2/3 and IC 2/4, this state remains until the next ALE pulse arrives.

- Read operation:

  The data on the read bus (LDB) are switched through to the processor (PDB) by the driver IC 17/2 IC 18/2 when an RAM position on the CPU motherboard or an input port is addressed. The RD strobe, which initiates the read operation in the RAM-ICs, has an advanced leading edge compared with the RD strobe. The trailing edge of the ALE pulse sets IC 28/1 if S1 = 1 (read status). If one of the RAMs is addressed, then the RD' strobe is generated via IC 25/1 and the addressed RAM becomes active. The trailing edge of the RD strobe sets IC 28/2. This resets IC 28/1 and RD' disappears. IC 28/2 is reset by each ALE pulse and set by the trailing edge of each RD strobe. When the measuring set is switched off, the RAM is supplied with voltage from an accumulator, thus retaining its contents. During this period, the RAM is protected against inadvertent write operations by the signal $\overline{\text{RESET IN}}$.

9.2.1.3 Interface to the IEC bus interface

If an I/O address of the IEC Bus Interface is addressed ($\overline{V_2}$ = low, IO/$\overline{M}$ = high), the drivers IC 26 or IC 27 are switched through to the read and write bus, respectively, of the RAM. The activation is carried out respectively with the RD strobe or the stretched WR strobe, which is generated with IC 2, as for the RAM.

9.2.1.4 Coupling the I/O area to the buses of the RAM area

When an I/O operation which does not address the IEC Bus Interface is executed, the output of IC 30/2 is low. In this case, the addresses are switched through from the RAM area to the I/O area (IC 35) and the data are switched through with the WR strobe (IC 32). In the case of an input command, the data to be read are buffered by the timing control in latch IC 31 and are switched through to the read bus by the RD strobe.

9.2.1.5 Timing control (IC 44 to IC 48)

The following timing diagram applies to input/output operations:

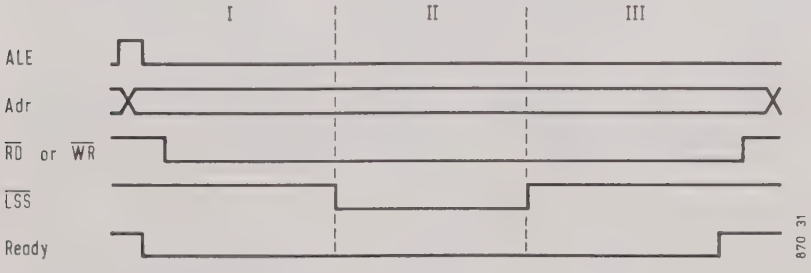


Figure 9-3 Basic timing in I/O area

This considerably slower sequence is necessary in order to provide the CMOS buses with sufficient time to assume the appropriate logic state.

The purpose of the timing control is to stop the computer with a Ready Signal for a sufficiently long period, to divide this period into three approximately equal sections, and to generate a low speed strobe, LSS. This reduction in the speed depends on the address of the port, as the various parts of the bus operate at different speeds.

Details of the timing control:

The ALE signal resets the flip-flops IC 46/1, IC 46/2, and IC 48/2. As soon as a port address which does not lie in the area V_0 is activated, the READY signal now becomes low (IC 47/2 and IC 47/3). The counter IC 45 is set to a value which determines the lengths of the various sections by the address decoder signals $\overline{V_1}$ and $\overline{V_3}$ coming from the CPU board. The clock, which is released via IC 44/3 by READY, sets IC 46/1 such that the counter can run. As soon as an overflow occurs in the counter, the next negative going edge sets IC 46/2 and the next second edge resets IC 46/1, which means that the counter can be reloaded. The same signal transition also resets IC 46/2, which means that IC 46/1 is again set with the next transition and the counter again starts to run (see Figure 9-4). When IC 46/2 is reset, IC 48/1 is set and $\overline{LSS}$ switches to low. At the next counter overflow, IC 48/1 is reset ($\overline{LSS}$ switches to high) and IC 48/2 is set. The third and last counter overflow only sets IC 46/2, thus switching the READY signal to high. The computer is again free to run and operates at its normal speed until the next I/O operation is started.

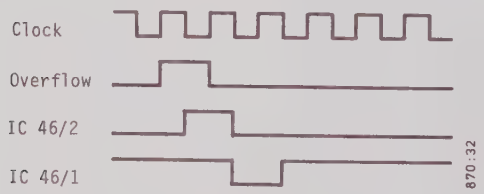


Figure 9-4 Overflow of counter IC 45

The IEC Bus Interface can stretch the $\overline{LSS}$ as long as required by means of the signal "IEC ready". This intervention is carried out via IC 44/4, and prevents IC 46/2 and IC 48/1 from changing state if $\overline{LSS}$ is low. IC 46/1 is therefore reset and prevents further operation of the counter via the set input.
IC 47/1 performs only a safety function.

Purpose of this arrangement:
During Section I of the sequence, the addresses settle and the predecoder completes decoding so that the correct port is activated in Section II. During Section II, the data on the data bus settle and should be stable by the time the trailing edge of LSS is reached. In Section III, the addressing logic has time to switch off the previously selected port. Only when this has been done are changes of state on the address lines permitted.

Just as the data on the processor bus are valid after the trailing edge of the $\overline{RD}$ or $\overline{WR}$ signal on the data bus, they are valid in the I/O area after the trailing edge of the $\overline{LSS}$ signal. The signals $\overline{WR}$ and $\overline{RD}$ are also used as $\overline{RD_C}$ and $\overline{WR_C}$ as status signals, i.e. for write/read switching.

9.2.1.6 Interface to the front panel

When the processor addresses a port of the front panel, the signal $\overline{V_1}'$ becomes low. This activates the address driver IC 55 and the data driver (IC 52, 53, 54) can be switched by the data strobes $\overline{RD}$ and $\overline{WR}$. The data strobes for the front panel $\overline{RF}$ and $\overline{WF}$ are generated from the control signals together with $\overline{LSS}$.

9.2.1.7 Frequency divider IC 49

IC 49 is a preliminary frequency divider for various clock signals which are required on the front panel.

9.2.1.8 Address decoders IC 56, 59, 60, 61

The predecoder signal $\overline{V_3}$ and the address lines IOA_2 to IOA_5 are decoded with IC 59/1 and IC 60/1. Decoding of IOA_0 and IOA_1 is carried out in IC 60/2, IC 61/1, and IC 61/2. IC 60/2 is opened for reading and IC 61/1 for writing during $\overline{LSS}$ = low, IC 61/2 is open for reading and writing. This means that the outputs of IC 61/2 do not drive ports in the normal sense and that the data on the data bus during these write/read operations are not evaluated by the processor.

The circuit utilizes only the pulse which results from addressing of the "virtual" ports. The same applies to the signal WCØ. Decoding of A_0 and A_1 is carried out by IC 58 (8255 A) on the chip itself.

9.2.1.9 Data interface to the SPM-19

The data interface is a bus interface to the processor system of the receiver SPM-19. The major part of the logic required for this is contained in 8255 (IC 58), which is programmed by the computer as follows:

Port A	Mode 2
Port B	Output mode 0
Port C (PC 0, PC 1)	Input

Further details of this can be found in the data sheet of the 8255.

Control from the SPM-19:
The generator has the address 0 (A_8 = 0, A_9 = 0) from the point of view of the receiver. Decoding is carried out by GL 1 and GL 2 on board 870-S (AMP socket). When the receiver wishes to transfer data to the PS-19, the signal $\overline{STB_A}$ (PC 4) is generated with the aid of the signals $\overline{PWR}$ and $\overline{PA}$, and the data are placed in IC 58. The signal IBF generates an interrupt RST 5.5 in the processor of the PS-19 via GL 6. In the opposite direction, the processor can generate the signal $\overline{OBF}$ in IC 58 by writing the transfer latch. The processor of the receiver then generates the signal $\overline{PRD}$ and thus, via IC 57/2, the signal $\overline{ACK_A}$ (PC_6). The signal $\overline{INTR}$ is set and reset by software in the processor. The signal 5 V_{cc} coming from the receiver is high only when the receiver is connected and switched on. If this signal is low, IBF cannot trigger an interrupt RST 5.5 due to IC 57/3, Gl 6, and Gl 7. However, the interrupt can still pass through IC 62/3 and IC 56/1, depending on the position of the flip-flop IC 62/1 and IC 62/2.

The current status of S V_{cc} can be interrogated by the processor via PC 2 on the 8255.

A supply voltage in the PS-19 of > 0 V may occur via the CMOS inputs and outputs of the data interface, although the PS-19 is switched off. This can cause the drivers of IC 58 to assume an uncontrolled low resistance state on the interface. R 48 is provided in order to block this.

9.2.1.10 Input and output gates

The input and output ports are standard circuits which require no further description.

Input gate	Address	C 4	IC 54/2, IC 65
Output gate	Address	C 3	IC 67 , IC 68
Output gate	Address	C 2	IC 69
Output gate	Address	C 1	IC 70

The address decoders also decode a few addresses to which no gates are connected. These signals are used as pulses which can be controlled by software, for example, addresses CØ, CC, ...

9.2.1.11 Voltage monitor for accumulator IC 73

Shortly after the power-on sequence, the voltage appearing at C 20 is the RAM that supplied just before the power was switched on. This is compared with a reference voltage (R 38, R 39) of approximately 2.3 V and the result made accessible to the computer via IC 72/3 and IC 58.

9.2.1.12 Power ON and power OFF logic

Due to the use of the non-volatile RAM, special measures are necessary during the power on and power off sequences of the processor.

As long as the unit is switched off and, above all, during the power on sequence and power off sequence of the supply voltage, the RAM is protected against inadvertent access by the signal $\overline{\text{RESET IN}}$. R 26 ensures that $\overline{\text{RESET IN}}$ remains at a low level, even without a supply voltage connected.

When the unit is switched on, the complementary flip-flop IC 74/2 and IC 74/3 remains in the off state even while the voltages are rising. IC 74/1 thus remains blocked and $\overline{\text{RESET IN}}$ remains low. The Signal MAINS OFF[1.)] coming from the power supply unit results in the following sequence:

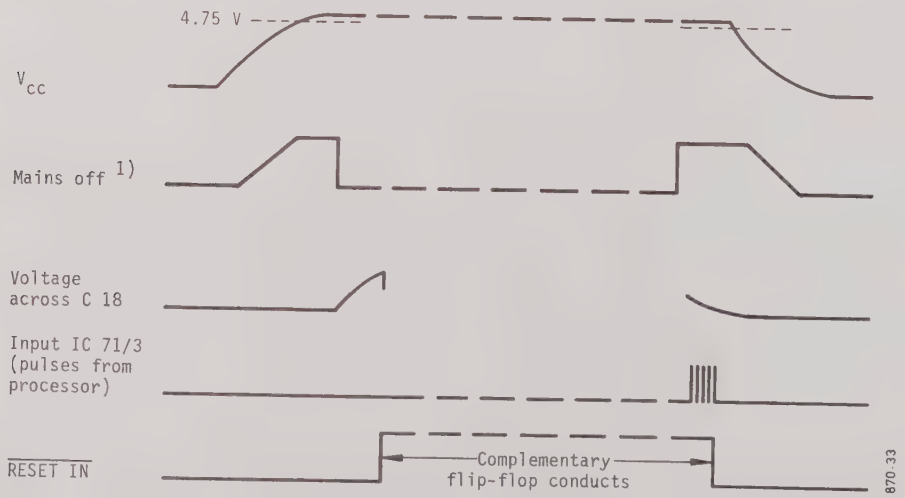


Figure 9-5 Power ON and power OFF logic

1.) called "Data Retention" in later documents

Approximately 30 ms after the supply voltage reaches its nominal range, MAINS OFF switches to low and the voltage across C 18 rises until IC 74/4 conducts. This causes the complementary flip-flop to conduct and $\overline{\text{RESET IN}}$ switches to high. The processor is simultaneously reset and starts to execute the program. In this state, 74/4 conducts in the inverse direction. When the PS-19 is switched off or if the mains supply fails, the signal MAINS OFF switches to high at least 2 ms before the supply voltage drops. An interrupt (TRAP) is triggered via IC 71/2 if the flip-flop IC 72/1/IC 72/2 is set. This flip-flop is reset for a max. of 1 ms by the software only for the duration of short program sections which must not be interrupted. At the end of the TRAP routine, the software generates as many pulses as required via IC 71/3 until the complementary flip-flop switches to the non-conducting state and the processor is stopped via $\overline{\text{RESET IN}}$. The case where the flip-flop does not switch to the off state with the first pulse can occur if the collector-base diode of IC 74/4 does not discharge capacitor C 18 sufficiently. For operation of the circuit, however, it does not matter whether one pulse or a maximum of approximately 50 pulses are required to change the state of the complementary flip-flop.

9.2.1.13 Interrupt line TRAP

The signal MAINS OFF is converted by IC 71/2 into the signal $\overline{\text{TRAP}}$. This is combined by open collector logic with the signal $\overline{\text{CLEAR}}$ from the IEC Bus Interface. The processor can interrogate the reason for the interrupt via gate PCØ on IC 58.

9.2.2 AMP SOCKET (6)

Circuit diagram 870-7506

This board is simply an adaptor from the ribbon cable to the AMP socket. The two diodes, together with R 11 on the CPU motherboard (870-7502), form a gate in negative logic, and which is used as an address decoder.

9.2.3 ADDER (24)

Circuit diagram 870-7524.014/33

The adder is addressed by the processor of the PS-19 as a group of output gates. Feedback is provided by the serial data input of the processor SID. It acts as an intelligent interface for control of the synthesizer.

Its precise function can be found in the description of the SPM-19, BN 829.

9.2.4 FRONT PANEL CONTROL (3)

Circuit diagram 870-7503

Circuit components, needed for the front panel circiutry, are mounted on this printed circuit board, because the area of the "Entry Circuit" p.c.b. in fully utilized. So no place is available for the mounting of these components.

9.2.4.1 Structure

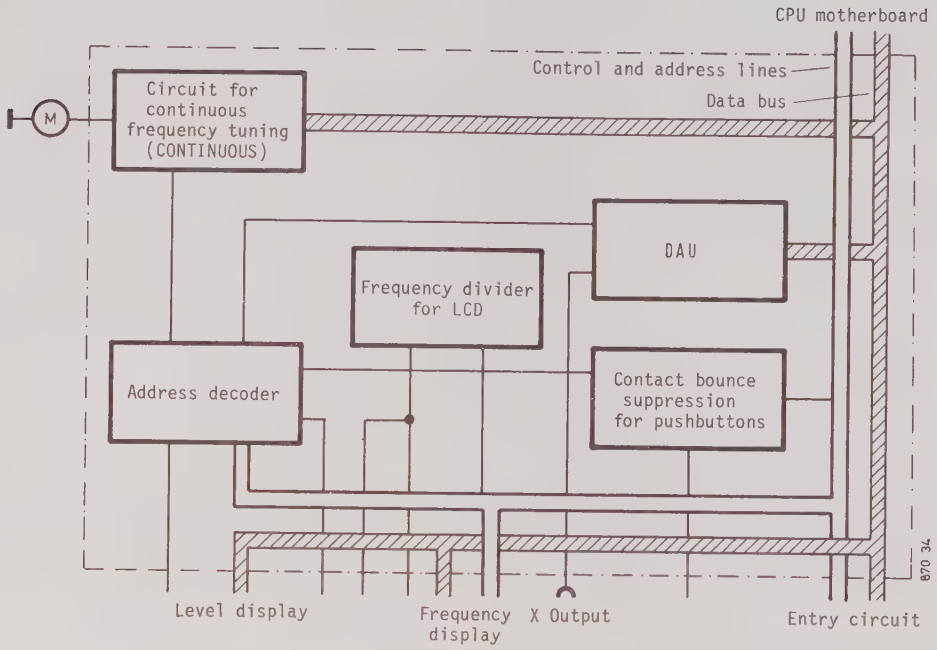


Figure 9-6 Structure of the front panel control

9.2.4.2 "CONTINUOUS" (IC 13 to IC 21)

Principle: When the motor generates a voltage due to rotation of the tuning knob, C 29 is charged positively or negatively. This causes the output of IC 12 to switch to its maximum value in one or the other direction. This, in turn, either prepares IC 15/1 via IC 13/1 for setting or prepares IC 15/2 via IC 14/2 for setting. As soon as a positive clock transition sets one of the flip-flops, T 1 or T 2 conducts for one half of the clock cycle via IC 14/4 or IC 16/2. This partially or completely drains the charge from C 29. If the charge is not completely drained, the cycle is repeated until the voltage across C 29 drops below a specific threshold.

The number of pulses available at the output of IC 6/3 is thus proportional to the charge on C 29. Depending on whether the voltage across C 29 was positive or negative, flip-flop IC 13/2/IC 13/3 is set or not set respectively. This causes the direction of counting of counters IC 20 and IC 21 to be switched such that the counters are incremented if the motor is turned clockwise and decremented if the motor is turned anticlockwise. The current counter value is interrogated by the processor via gate address 50 (IC 18 and 19).

Details:

- If the motor is turned so rapidly that the resulting voltage becomes > 1 V, diodes GL 5 and GL 6 or GL 7 and GL 8 conduct. C 29 is then charged via R 34 (instead of R 32). The charge is thus disproportionally high.
- The output level of IC 16/2 is converted to the range - 5 V to 0 V by GL 4, C 30, and R 35, such that T 1 and T 2 are driven with a completely symmetrical signal.

- If the voltage across C 29 = 0 V, the output of IC 12 is set to 2.5 V. The voltage divider R 21 to R 24 ensures that 0 V or 5 V, respectively, is then present at the gate inputs. If the output voltage of IC 12 is at its maximum positive value, then the logic levels of both connected gates are high, and vice versa for the maximum negative voltage.
- In order to ensure that the processor can always read the contents of the counter correctly, it must be possible to interrupt the counting operation by means of the software. This is made possible by setting Latch 3 (output Pins 11 and 12) in IC 17 (output gate, address 48).
- For testing purposes, the flip-flops IC 15/1 and IC 15/2 can be permanently set or reset. This is done by software via IC 17, Latches 2 and 3, and via IC 14/1 and IC 14/3. This causes a maximum number of pulses to be counted into the counter and C 29 to be charged accordingly.
- As soon as one of the flip-flops IC 15/1 and IC 15/2 is set for the first time, IC 3/2 is also set. This initiates an interrupt in the processor via IC 13/4 if Latch 1 in IC 17 is set.
- IC 3/2 can be reset by software by selecting the address 52. This is done after the counter value has been read. When IC 3/2 is reset, the counter is set to the value of 50 (IC 20 to Ø, IC 21 to 5). The counting operation thus always starts at 50.
- If the counter reaches a maximum value (ØØ or 99), then the overflow bit of IC 21 switches to low. This interrupts the counting operation with IC 6/3.
- The following information is accessible to the processor via address 51 (input gate IC 18):
  1.) Counter has overflowed
  2.) Position of IC 3/2

The remaining bits of gate 51 are used for the pushbuttons of the input circuit.

9.2.4.3 Contact bounce suppression circuit, IC 1 to IC 3

The contact bounce suppression circuit used here is a so-called adaptive suppression circuit: the suppression time is increased to match the contact bounce time.

The signal T 6 (pushbutton depressed) indicates whether a pushbutton in a valid column of the pushbutton matrix has been depressed.

If no pushbutton is depressed, then T 6 = low. Counter IC 1/1 is therefore not reset (IC 2/4, IC 2/1) and thus counts up until it reaches the state 8. Here, Q 8 (Pin 6) becomes high and the counting operation is interrupted via Pin 1 (clock). The other counter IC 1/2 is reset via IC 2/3.

When a pushbutton is depressed:
TG switches to high. IC 1/2 is no longer reset and starts to run. As soon as a contact bounce pulse appears, it is temporarily reset. This resetting is repeated until there has been no contact bounce for approximately 22 ms, which means that the contact is certainly closed.

This occurs when the counter reaches the state 8 ($Q_3 = 1$) and initiates the following operations:

- The counting operation is stopped (Pin 9 = clock becomes high)
- IC 1/1 is reset via IC 2/4 and IC 2/1 because T 6 = high.
- This means that IC 1/2 can no longer be reset by contact bounce pulses, due to IC 2/3 and IC 2/2.
- IC 3 is set and initiates an interrupt in the computer via IC 4/1.

This state remains stable until the pushbutton is released.

When a depressed pushbutton is released again:
TG switches to low. IC 1/1 is no longer reset and starts to run. As soon as a contact bounce pulse appears, it is again temporarily reset. This resetting is repeated until no bounce pulse appears for approximately 22 ms, which means that the contact is certainly open. At this point, the counter IC 1/1 has reached the state 8 ($Q_3 = 1$). The state "no pushbutton depressed" has now been reached (see above), and IC 1/2 is reset.

IC 3/1 is reset under software control with the same pulse as used for IC 3/2.

9.2.4.4 Address decoders IC 7 to IC 9

The circuit itself is a standard circuit and requires no further explanation.

The input signals:
The data strobes $\overline{RF}$ (read front panel) and $\overline{WF}$ (write front panel) become low approximately 2.5 ms after the addresses are applied. The pulse duration is also approximately 2.5 µs. The addresses remain stable for approximately 2.5 µs after the end of the strobe. The strobes are activated only when a gate of the front panel area is actually addressed.
In the case of IC 9, it should be noted that only Motorola or RCA circuits may be used!

9.2.4.5 Digital-analog converter IC 10 and IC 11

The circuit containing IC 10 and IC 11/2 is a standard application (see data sheet).
IC 11/1 acts as a voltage follower for the reference voltage of -7.5 V produced by R 4 and R 5.
R 7 and R 10 divide the DAC output voltage present at the output of IC 11/2, such that the available voltage range at the socket is -2.5 V to +2.5 V.

9.2.5 ENTRY CIRCUIT (4)

Circuit diagram 870-7504

9.2.5.1 Address decoder IC 4, IC 5

The circuit itself requires no further explanation (standard).
The signal $\overline{EWR}$ switches to low for approximately 2.5 µs after the addresses have settled and when an output gate of the entry circuit is addressed.
The read signal for the input gate with address 53 (IC 3) is decoded on the board "front panel control".

9.2.5.2 Pushbutton matrix

The columns of the pushbutton matrix are driven by the output gates 44 and 45 (IC 6 and IC 8). The lines can be interrogated by the processor via the input gate 53 (IC 3).

In the idle state, all columns in which pushbutton operations are to be accepted are set to low by the software. The lines are pulled to high by IC 2, and signal TG (pushbutton depressed) is low.

If a pushbutton in one of the active columns is now depressed, the corresponding line switches to low and the signal TG switches to high. This initiates an interrupt in the processor via the contact bounce suppression circuit. The processor now resets all columns except for one to high and interrogates the lines via gate 53. If all lines are high, then the pushbutton which was operated was not in the active column. All columns are now searched until the actual pushbutton which was depressed is found.

If, in the idle state, a column is not set to low, i.e. is not active, depression of a pushbutton in this column does not initiate an interrupt, and depression of the pushbutton has no effect. The diodes GL 1 to GL 10 and the resistors R 2 to R5 and IC 7 are required for the case where several pushbuttons in the same line are depressed simultaneously. Without the diodes, the outputs of the column drivers would otherwise be short-circuited to each other.

9.2.5.3 LED control circuit

The LEDs are driven directly or via decoders via output gates IC 10, 11, 13, 14, 17, and 18. If a decoder or the software control ensures that only one of a group of LEDs can light, a common dropping resistor is used.

9.2.6 LEVEL DISPLAY (5)

9.2.6.1 Circuit diagram 870-7505

The ICs which drive the liquid crystal display also contain the output gates. Address decoding is carried out on the board "front panel control".
Data bus: PEDX Selection signals: PEAXX

9.2.6.2 Level display (LED) (5)

PS-19: Series D ...

The data (PEFD0 ... PEFD7) passes from the CPU mother board along the data bus to the latch inputs (IC 4, 5, 7, 9, 10). The addresses PEA4B ... PEA4F then select those latches which are to receive data. The counter (IC 1) is driven and incremented by the clock signal from the frequency display. The latches (IC 4, 5, 6, 7, 9, 10) and the appropriate digit drivers as addressed in parallel via the decoder (IC 2). The outputs of the addressed latches change from the tristate to the state determined by the incoming data. In this way a 4 bit data block is passed to the internal "segment bus" via the segment drivers (IC 19, T1 ... T7).

The decimal point is driven via IC 18.

IC 11, 12 and 13 decode the unit information which has been written to IC 10. The characters ⇩ , ⇧ , - and + are driven directly from the appropriate bits with the help of the power elements in IC 16, 18. The DA converter built up around drives the transistor T9. This part of the circuit adjusts the current, so that a constant current is always drawn from the whole circuit for the power supply.

Digit selection:

Counter state IC 1				Activated latch	Activated digit
Q_4	Q_3	Q_2	Q_1		
L	L	L	L	IC 7.1	IC 29
L	L	L	H	IC 7.2	IC 28
L	L	H	L	IC 5.1	IC 27
L	L	H	H	IC 5.2	IC 26
L	H	L	L	IC 4.2	IC 25

9.2.7 FREQUENCY DISPLAY (19)

Circuit diagram 870-7519

9.2.7.1 LCD display

The ICs which drive the liquid crystal display, IC 4 to IC 16, also contain the output gates. The digits are driven via the data bus FRD Ø to FRD 3, and the decimal points via the data bus line FRD 7 and the decimal point logic. The unit "kHz" is activated by an external gate. For this reason, the control signal is connected statically via the ribbon cable.

9.2.7.2 Address decoder IC 4

Standard circuit
It should be noted that only Motorola or RCA circuits may be used.

9.2.7.3 Decimal point logic IC 3

If the kHz display is off (signal FRKHZ low), IC 3/3 acts only as an inverter and the decimal points can be controlled as required by the software.

If the kHz display is on, the processor always issues bit 7 (FRD 7) as "1". During subsequent output of the digits, the decimal points DP 4 and DP 7 are automatically set and all others reset.

9.2.7.4 Frequency display (LED) (19)

PS-19: Series D ...

The 4-bit data block (FRDØ ... FRD3) passes along the data bus to latches (IC 4, 5, 7, 10, 17). The appropriate latches are selected and the data stored in them via the address bus (FRA8 ... FRA10) and the decoder (IC 1).

IC 16 operates as an astabile multivibrator. The appropriate latches and digit drivers T11 ... T18 are driven in parallel via the counter IC 15 and the decoder (IC 14).

The information from the selected latch goes to the decoder (IC 9), where it is recorded for 7 segments. It then goes to the driver (IC 8; T2 ... T9) on the internal "Segment" bus.

The D/A converter built up around IC 6 and IC 8 draws the required amount of current via T1 so that the circuit behaves for all contacts and purposes like a constant load on the power supply.

The decimal point goes via FD7 and IC 3 to the addressable 8 bit latch (IC 12) depending on the address (PRA8 ... FRA10) the information multiplexer (IC 17) to the decimal point positions.

9.2.8 APPENDIX

Bit assignments of I/O gates in the PS-19

Designation	Label/ address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ALC (Reference -attenator):										
Output-Attenuator	OUTATT C 1	0	1.)	20 dB#3 OAC	20 dB#2 OAC	20 dB#1 OAC	10 dB OAC	5 dB OAC	5 dB FAC	1.)
Ref.-Attenuator	REFATT C 3	0	Blanking	-4 dB	-2 dB	-1 dB	-0.8 dB	-0.4 dB	-0.2 dB	-0.1 dB
Control signals dBm-Corr. and Generator off	STESIG C2	0	1.)	ST 1	ST 2	Used by UBERPE!	Fast time constant	1.) →		
				0	0	≅ 0 dB				
				0	1	≅ +0.03 dB				
				1	0	*) see below				
				1	1	≅ -0.04 dB				
Mixer: Carrier Control	AUSGAN C 9	0 (J)	Carrier Switching external	Signal on		Used by AUSGAN, see below				
Output: Output switch	AUSGAN C 9	0 (I)	Used by T R A E S T see below		Rel 6/7 620 kHz 150 Ω	Rel 5 koax 75 Ω	Rel 4 14 MHz bal. 124 Ω	Rel 3 150 Ω	Rel 2 620 kHz bal. 600 Ω	Rel 1 0 Ω
Increased level +10 dB	STESIG C 2	0	1.)	Used by STESIG!		+10 dB increased level	1.) →			

*) Signal BLANK (digital blanking, -20 dB), is not used by the software. It is provided for a later version of the AGC amplituder for "20 Hz switching".

Table 9-1 Control gates of signal; bit assignments

1.) These bits are not used in output gates.
A "1" is always read from this position in input gates.

2.) These bits of input gates contain any data, which are explained elsewhere.

3.) Activation of this gate (read or write or possibly both) executes the specified function.
Data as for 1.).

Designation	Label/ address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data (read and write)	Data C 8	IO	D a t a b y t e							
Handshake signals	CA	I	$\overline{OBF}$	$\overline{INT}$ (for SPM)	IBF	Ø	Unde-fined	SPM on (5 V_{cc})	2.)	2.)
Control words										
Initialization requests (Mode 1)	CONTRO CB	0	1	0	1	1	1	0	0	1
Working mode (Mode 2)			1	1	1	1	1	0	0	1
Reset interrupt (in Mode 2)			0	1	1	1	1	1	0	1
SPM-Vcc interrupt:										
Enable	CC	IO	3.) ———							
Disable	CØ	0	3.) but only write is possible							

Table 9-2 Data interface to SPM-19; bit assignments

Designation	Label/ address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Enable TRAP	CF	IO	3.) ———							
Disable TRAP	CD	IO	3.) ———							
Activate reset	CE	IO	3.) ———							
Check accumulator voltage	CA	I	2.) ———						Voltage suffi.	2.)
TRAP status RAM (Mains off/interface clear)	CA	I	2.) ———							Mains off

Table 9-3 Control gates for data maintenance and reset; pin assignments

---

1.) These bits are not used in output gates.
A "1" is always read from this position in input gates.

2.) These bits of input gates contain any data, which are explained elsewhere.

3.) Activation of this gate (read or write or possibly both) executes the specified function. Data as for 1.).

Designation	Label/ address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Continuous:										
Continuous-counter	5Ø	I	BCD counter value				BCD			
			8×10^1	4×10^1	2×10^1	1×10^1	8×10^0	4×10^0	2×10^0	1×10^0
Front panel status	51	I	1.) →		key depressed	Cont. counter carry	1.) →		Continuous interrupt	Key board interrupt
Reset for continuous interrupt, Continuous counter and keyboard interrupt	52	I	3.) →							
Continuous-control	CONSTE 48	0	Enable cont.-interrupt	Test continuous	Counter stop	Used by FREKHZ	1.) →			
DAU:										
DAU LSB	4A	0	Data byte D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DAU MSB	49	0	D_9	D_8	1.) →					
			The DAU/MSB must be transmitted before the LSB							
Programming switch										
Measuring matching and test	C4	I	*) Z_1	*) Z_2	DEFAULT*) intia-lization	*)	Open=Test closed = run	1.)	1.)	2.)
			Switch No. 1	2	3	4	5			
Switch:										
Rear switch	C4	I	2.) →					1.) →		0 ≙ dB 1 ≙ dBm

*) Switch closed = 0 = active. This meaning of the switch is valid only if S5 is closed (run).
In the case of test (S5 open), these switches are used for selection of test programs.

Table 9-4 Gates for "continuous" DMU, program switches and rear switch; pin assignments

1.) A "1" is always read from this position in input gates.

2.) These bits of input gates contain any data, which are explained elsewhere.

3.) Activation of this gate (read or write or possibly both) executes the specified function. Data as for 1.).

Designation	Label/ address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pushbutton:										
Column, group A	SPALTA 45	0	1.) →		Column 0	Column 1	Columnn 2	Column 3	Column 4	Column 5
Column, group B	SPALTB 44	0	1.) →				Column 9	Column 8	Column 7	Column 6
Lines	53	I	1.) →		Line 5	Line 4	Line 3	Line 2	Line 1	Line 0
Front panel status (see continuous)	51	I								
Reset pushbutton interrupt (see Continuous)	52	I								
LEDs:										
Output, Z-values etc.	TLO OUT 42	0	1.) →				For definition see next sheet O_3	O_2	O_1	$O_\emptyset$
Single-LEDs in Level-section	TLD PEG 41	0	1.) →		see next sheet DE_1	DE_0	see next sheet dB_1	dB_0	*) dBr0	*) BLANK
RATE/S	TLD RAT 40		1.) →				For definition see next sheet R_3	R_2	R_1	R_0
Frequency-LEDs Entry and display	TLD FRE 47	0	1) →		*) f	*) f_{CENT}	*) f_{STOP}	*) f_{START}	*) f_{STEP}	*) f
Single-LEDs in Frequency section	TLD BET 46	0	1.) →		*) REMOTE	*) EXT	For definition see next sheet F_3	F_2	F_1	F_0
LED "AUTO BLANK"	TLD BLA 43	0	1.) →							AUTO *) BLANK

*) $\emptyset$ = LED on, 1 ≙ LED off

Table 9-5 Pushbuttons and LEDs; bit assignments

1.) These bits are not used in output gates.
A "1" is always read from this position in input gates.

2.) These bits of input gates contain any data, which are explained elsewhere.

3.) Activation of this gate (read or write or possibly both) executes the specified function.
Data as for 1.).

Output LEDs:

O_3	O_2	O_1	$O_\emptyset$	LED inscription
0	0	0	0	coax. 75Ω
0	0	0	1	124 Ω
0	0	1	0	150 Ω BAL. I
0	0	1	1	150 Ω Z
0	1	0	0	150 Ω 0
0	1	0	1	600 Ω Z BAL. II
0	1	1	0	600 Ω 0
0	1	1	1	(All
1	X	X	X	off)

dB LEDs:

dB_1	$dB_\emptyset$	LED inscription
0	0	dB
0	1	dBmO
1	0	dBm
1	1	(all off)

Rate LEDs:

R3	R2	R1	RO	LED inscription
0	0	0	0	Manual sweep
0	0	0	1	300
0	0	1	0	100
0	0	1	1	30
0	1	0	0	10
0	1	0	1	3
0	1	1	0	1
0	1	1	1	0.3
1	0	0	0	0.1
1	0	0	1	0.03
All other combinations				(All off)

Digital ENTRY SELECT:

DE1	DE0	LED inscription
0	0	FREQ
0	1	MEM
1	0	LEVEL
1	1	All off

F3	F2	F1	F0	LED inscription
0	0	0	0	FINE
0	0	0	1	COARSE
0	0	1	0	STEP
0	0	1	1	SWEEP
0	1	0	0	SWEEP ⌜
All other combinations				(All off)

Table 9-6 1 out of N tables for LEDs; bit assignments

	SPALT A						SPALT B			
Bit No. / Column / Line No. / No.	(4) 0	(5) 1	(6) 2	(7) 3	(8) 4	(9) 5	(3) 6	(2) 7	(1) 8	(0) 9
0	Level-steps -0.1 dB 20 H/64	dBm0 28 H/80	(comma) , 30 H/96	8 38 H/112	MEM 40 H/128	/	STEP ⇩ 18 H/48	f_{STEP} 10 H/32	/ ØB H/16	/ ØØ H/0
1	Level-steps +1 dB 21 H/66	dBr 29 H/82	(minus) — 31 H/98	9 39 H/114	FREQ 41 H/130	CLR 49 H/146	MAN 19 H/50	f_{START} 11 H/34	/ Ø9 H/18	LOCAL Ø1 H/2
2	Level-steps -10 dB 22 H/68	BLANK 2 AH/84	3 32 H/100	6 3AH/116	dBm/dBm0 42H/132	AUTO-BLANK 4AH/148	SWEEP ⌠ 1AH/52	Δf 12H/36	RATE ØAH/20	/ Ø2H/4
3	Level-steps +0,1 dB 23 H/70	dBm 2BH/86	0 33H/102	7 3BH/118	LEVEL 43H/134	/	STEP ⇧ 1BH/54	f 12H/38	/ ØBH/22	/ 03H/6
4	Level steps +10 dB 24H/72	Z_{out} switch ⇦ 2CH/88	2 34H/104	5 3CH/120	kHz/RCL 44H/136	/	SWEEP 1CH/56	f_{CENT} 14H/40	RATE ⇨ ØCH/24	/ Ø4H/8
5	Level-steps -1 dB 25H/74	Z_{out} switch ⇨ 2DH/90	1 35H/106	4 3DH/122	MHz/STO 45H/138	/	AUTO-STEP 1DH/58	f_{STOP} 15H/42	EXT ØDH/26	/ Ø5H/10

Branch table address — Branch table position

Table 9-7 Pushbutton matrix; gate assignments

Designation	Label/ address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sign, decimal points, arrows, half position	PEG VORTB 4E	0	1.)	DP 1 (first from right)	⇧	⇩	*)	−	DP 2 (second from right)	Half-position figure "1"
Position 3 and Position 4	STE3U4 4D	0	Position 4	B	C	D	Position 3	B	C	D
Position 1 and Position 2	STE1U2 4C	0	Position 2	B	C	D	Position 1	B	C	D
Unit	PEGDIM 4B	0	Di_7	Di_6	Di_5	Di_4	Di_3	Di_2	Di_1	Di_0

See table below

Unit display

Display	Di_7	Di_6	Di_5	Di_4	Di_3	Di_2	Di_1	Di_0	in Hex
dB	0	0	0	0	0	0	0	1	Ø1
dBO	0	1	0	0	0	1	1	1	47
dBOp	0	1	0	1	0	1	1	1	57
dBr	0	0	0	0	0	1	0	0	Ø4
dBm	0	0	1	0	1	0	1	1	2B
dBmO	0	1	1	0	1	1	0	1	6D
dBmOp	0	1	1	1	1	1	0	1	7D
pWO **)	0	1	0	0	0	0	1	0	42
pWOp **)	0	1	0	1	0	0	1	0	52
Blank	0	0	0	0	1	1	1	1	ØF

*) The minus sign must be activated separately

**) DP 3 appears simultaneously

Table 9-8 Level display; bit assignments

1.) These bits are not used in output gates.
A "1" is always read from this position in input gates.

2.) These bits of input gates contain any data, which are explained elsewhere.

3.) Activation of this gate (read or write or possibly both) executes the specified function.
Data as for 1.).

Designation	Label/ address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100 MHz digit	4F	0	*) dec. pt.	1.) →			B C D only 1 or blank possible			
10 MHz digit	58	0	*) dec. pt.	1.) →			B C D			
1 MHz digit	59	0	*) dec. pt.	1.) →			B C D			
100 kHz digit	5A	0	*) dec. pt.	1.) →			B C D			
10 kHz digit	5B	0	*) dec. pt.	1.) →			B C D			
1 kHz digit	5C	0	*) dec. pt.	1.) →			B C D			
100 Hz digit	5D	0	*) dec. pt.	1.) →			B C D			
10 Hz digit	5E	0	*) dec. pt.	1.) →			B C D			
1 Hz digit	5F	0	*) dec. pt.	1.) →			B C D			
Units kHz	CONSTE 48	0	Used by CONSTE			"kHz" display	1.) →			

*) The decimal point must be switched on with "Ø"
This function applies only as long as the kHz display is off. As soon as the display is on, the bit for the decimal point must always be transmitted as "1". The decimal points are set by hardware when all digit positions are filled with the correct information.

Table 9-9 Frequency display; bit assignments

9.2.11 40 MHz OSCILLATOR AND PHASE CONTROL LOOP (11)[4)]

Circuit diagram 870-7511.014/33

9.2.11.1 Introduction

The signal frequency (40 MHz) is generated in an LC oscillator. This is coupled to a precise and spectrally pure reference frequency (10 MHz) via a phase control loop. The quality of the signal thus corresponds to the quality of the reference frequency.
The oscillator is followed by a low-pass filter in order to suppress any harmonic content.

1.) These bits are not used in output gates.
A "1" is always read from this position in input gates.
2.) These bits of input gates contain any data, which are explained elsewhere.
3.) Activation of this gate (read or write or possibly both) executes the specified function.
Data as for 1.).
4.) Sections 9.2.9 and 9.2.10 have been deleted.

9.2.11.2 40 MHz oscillator

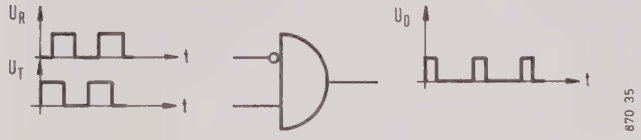
The LC oscillator is constructed as a colpitts circuit. Its main components are T_2, L_1, C_6, C_8, C_{10-12}, and $Gl_{3,4}$. It is tuned by a phase-dependent DC voltage on the control amplifier. In order to linearize the capacity voltage characteristic of the diodes, the control amplifier has a voltage-dependent load resistance (R_{21}, R_{19}, R_{22}, Gl_5). The signal is extracted via T1, which provides isolation.

It should be possible to gradually blank the oscillator signal. During this blanking operation, transistor T4 takes over the current of T1 in an almost linear manner as a function of time and drains it to ground. This time linearity is obtained by the Miller effect with the aid of capacitor C13 and transistors T4 and T5

9.2.11.3 Phase control loop

The isolating and amplifier stage consisting of T7 and T8, with DC negative feedback, is used to drive the 4:1 divider (SN 74 S 74). The divided oscillator frequency is compared with the reference frequency in the phase discriminator consisting of T_{11}, T_{13}, and T_{14}.

The phase discriminator also acts as a limiter. Its function can be regarded as a digital AND circuit with an inverting input:



The phase-dependent voltage is available at the collector of transistor T_{11}. It is smoothed with C_{26} and on the filter circuit between the emitters of transistors T_{15} and T_{16} removes the reference frequency and its harmonics. This is followed by the control voltage amplifier T_{16}, via which the control voltage is returned to the oscillator with the correct level. The supply voltages are additionally filtered in the oscillator and the phase control loop in order to prevent the power supplies from affecting the amplitude and phase.

9.2.12 40 MHz LOW-PASS FILTER (12)

Circuit diagram 870-7512

This is a ∞ /1 ninth order Chebyshev low-pass filter with a theoretical ripple of 0.18 dB. Its limit frequency is 44 MHz. The low-pass filter is fed by the collector of the isolating stage in the oscillator and is terminated (150 Ω) by the mixer input.

9.2.13 LIMITER AND MIXER (13)

Circuit diagram 870-7513

The assembly "limiter and mixer" consists of the two boards "limiter" (870-H) and "mixer" (870-G), which are mounted in separate screening cases in order to reduce interference to a minimum. The limiter board can operate alone, while the mixer board requires the bias voltage generation circuit on the limiter board.

The carrier signal (40 ... 65 MHz) passes through a high-pass filter (C 1, C 2, L 2, L 3) to a three stage limiter and driver circuit consisting of IC 1 and T 3, T 4. A square wave signal of approximately 1 V_{pp} is available at the collectors of T 3 and T 4. Transistors T 1 and T 2 provide temperature-compensated bias voltages for the limiter and the mixer.

The mixer is an active switching mixer in which the mixer transistors T 6, T 8, T 9, T 11 switch the currents coming from the current source transistors T 7, T 10 at the rate of the carrier signal. A low distortion 40 MHz signal frequency is superimposed on the currents through T7 and T 10. The transformer UE1, together with the symmetrical circuit design, provides good common mode rejection. The diode Gl 1 is a PIN diode which normally carries a direct current and thus has low resistance. When the signal frequency is blanked, the direct current through Gl 1 also drops to 0, thus providing high blanking attenuation for the signal frequency.

9.2.14 25 MHz LOW-PASS FILTER (14)

The 25 MHz low-pass filter is a ninth order filter approximated by a computer in accordance with the existing tolerance plans.

The input and output impedances are $Z_{in} = Z_{out} = 150\ \Omega$. The actual filter is preceded by an auxiliary low-pass filter in order to fulfill the high attenuation requirements at frequencies up to 500 MHz.

The actual filter is followed by an attenuator of 0.5 dB, then a further low-pass filter whose output capacitance is formed by a 9 cm length of subminax cable (connection to the next assembly). In order to fulfill the high attenuation requirements, to avoid mutual coupling between the coils, and to ensure direct contact to ground, the filter is installed in a six chamber screening case: the first chamber contains the auxiliary low-pass filter, the second to fifth chambers the filter, and the sixth chamber the attenuator and matching low-pass filter.

Repair or adjustment of the filter is possible only under the conditions specified in the testing regulations.

9.2.15 AGC AMPLIFIER (15)

Introduction

The AGC amplifier is an amplitude control circuit, stabilized by a feedback loop, which has a bandwidth of 80 Hz to 25 MHz. At an input level of -25 dB, the circuit can generate an output level of +10 dBm to -74.9 dBm over the whole frequency range. The extremely precise output level and the flat frequency response result from the extremely precise 20 kHz reference level and precision, wideband attenuators. The control loop, with a high degree of negative feedback, operates with two switchable time constants. The normal time constant is used for frequencies above 10 kHz and reacts rapidly to changes of the input level. The longer time constant is used for frequencies less than 10 kHz.

The AGC amplifier not only offers high accuracy under normal operating conditions, but can also process swept input frequencies. In such cases, the circuit must not only react to changes in the input level, but must also compensate for the intrinsic frequency response of the signal path. For this reason, the signal path must have a very good frequency response over the whole bandwidth, independent of the automatic control.

Function and principle of operation

As can be seen from the block diagram in the Appendix the module can be divided into 9 circuits. The RF section consists of the variable amplifier (1), output amplifier (2) and wideband attenuator (3). The negative feedback path consists of the loss-simulation circuit (4) and the follow-up rectifier (5). The reference signal for the data feedback loop is generated by the 20 kHz reference generator and passes through the precision reference divider (7). This signal is then fed to the follow-up rectifier (5). The regulation circuit (9) operates with the amplified differential voltage of the follow-up rectifier, generates the necessary loop gain, and thus determines the stability and the settling behavior of the control loop. The output voltage of the control circuit is fed to the variable amplifier, where the signal is attenuated as required. The last circuit is relay control circuit (8), which generates the control signals for the relay-switched attenuation stages in the wideband attenuator and for the loss-simulation circuit.

The input signal is fed to the variable amplifier, where it passes through the controlling element, an electronically-controlled attenuator. The output signal of this attenuator is amplified in a low-noise amplifier and then passed to the final amplifier for further amplification. At the output of the final amplifier, the signal is connected to two terminated outputs. The signal of the first output passes through the wideband attenuator to the output of the AGC amplifier. The second output of the final amplifier is connected to the loss-simulation circuit. This circuit precisely simulates the insertion loss of the output attenuator and the external impedance switching which follows the AGC amplifier. In addition to a fixed 5 dB attenuator, a 5 dB attenuator can be connected if levels greater than +5.0 dBm are required at the output.

The output signal of the loss-simulation circuit is connected, together with the reference signal coming from the reference divider, to two terminated RMS rectifiers. These rectifiers are designed such that equal input levels result in equal voltages at the outputs, regardless of the frequency of the signal connected from the final amplifier to the two halves of the rectifier. Each half of the rectifier generates a DC voltage which is proportional to the RMS value of the input signal. The two DC voltages are connected to a differential amplifier, amplified and passed on to the control circuit. Here, the control voltage is either amplified or attenuated as a function of the selected time constant. Phase correction elements provide the stability and the necessary settling behavior of the negative feedback loop. The output voltage of the control circuit supplies the amplifier in the control element which, in turn, determines the attenuation of the control element. The negative feedback loop is thus closed.

For normal operations, the rectified signal from the loss-simulation circuit is compared with the rectified signal from the reference attenuator.

The amplified voltage difference generates a corresponding attenuation in the control element such that the output voltages of the two rectifiers become equal. Precise equality of the two rectifier halves indicates that the output level of the loss-simulation circuit has reached a value which is identical with that of the reference attenuator. As the frequency response of the loss-simulation circuit is also identical to that of the wideband attenuator and the external impedance switching, this means that the output signal is controlled precisely by the reference attenuator. As a result of this, the regulating effect of the negative feedback loop ensures that the output level of the instrument is precisely equal to that of the reference attenuator at any frequency within the operating range. However, this is not true if attenuator stages are inserted in the wideband attenuator or in the loss-simulation circuit.

Changes of the output level can be achieved in two ways: firstly, by changing the reference level with the reference attenuator and secondly by changing the attenuator settings of the wideband attenuator or feedback attenuator. The truth table shows all attenuator settings for various output levels. The reference attenuator provides an output level of 0 dBm to -4.9 dBm, which can be changed in steps of 0.1 dB. If it is assumed that the wideband attenuator is not connected in the circuit, and taking into account the fixed attenuation of 5 dB in the loss-simulation circuit, then the output level of the AGC amplifier varies between +5 dBm and +0.1 dBm when the output level of the reference attenuator varies between 0 and -4.9 dBm. The AGC amplifier is thus capable of generating an output level change of 4.9 dB in 0.1 dB steps, depending on the settings of the reference attenuator. As the truth table shows, the output attenuator can provide an attenuation of 75 dB in 5 dB steps.

The combination of reference attenuator and wideband attenuator generates a level of +5 dBm to -74.9 dBm, which can be varied in steps of 0.1 dB, at the output of the AGC amplifier. In order to generate an output level greater than +5 dBm, the switchable 5 dB attenuator in the loss-simulation circuit is activated. This causes the level at the final amplifier output to rise by 5 dB and permits, together with the range of the reference attenuator, level variation between +10 and +5 dBm.

As described above, the wideband attenuator and the fine steps of the reference attenuator generate an output level between +10 dBm and -74.9 dBm in steps of 0.1 dB. It should be noted that, when the 5 dB feedback attenuator is activated, a 5 dB gain step in the final amplifier is activated simultaneously in order to achieve the necessary increase of the output level.

As can be seen from the block diagram, the maximum gain of the signal amplifier stages is approximately 36 dB. For this reason, the attenuation of the control element must vary between approximately 10 and 15 dB, depending on the setting of the reference attenuator, at an input level of -25 dB. For variations of the input level of $\pm$3 dB, the control element must have a range of 7 to approximately 18 dB. In the position "blank generator", the output of the reference attenuator is blocked and a high control voltage is simultaneously injected into the control loop in order to set the attenuation of the control element to its maximum value of approximately 35 dB. The time constant, together with the blanking circuit, ensures that the signal is blanked and unblanked smoothly.

The control loop is equipped with two switchable time constants. In the normal operating mode, which is generally used for frequencies greater than 10 kHz, the bandwidth of the control loop is approximately 500 Hz. This provides rapid settling for changes in the input level and for changes in the reference attenuator setting. In the operating mode "large time constant", the loop bandwidth is reduced drastically to approximately 17 Hz. This ensures that the signal to be controlled remains undistorted, which would not be the case if the control loop were to follow the instantaneous voltage variations. The time constant of the loop is switched at two points.

Firstly, the filter capacitance on the signal side of the follow-up rectifier is increased in the operating mode "large time constant". Secondly, the networks for magnitude and phase in the control loop circuit are modified. For the normal time constant, a further change is initated, namely connection of a high-pass filter with the limit frequency of approximately 1.6 kHz at the input of the final amplifier. This filter prevents a rapidly changing control voltage from acting through the control element, propagating itself in the signal path and leading to instability of the control loop.

The above sections describe the function of the AGC amplifier and the various sections of the circuit. In the following sections, the various circuits are described in more detail.

9.2.15.1 Variable amplifier (1)

The variable amplifier consists of two parts. The first is the control element, electronically-adjustable attenuator divider which acts as the variable attenuation element of the control loop. The control element utilizes the effect of the small signal resistance at the PN junction of a diode

$$r_d = \frac{nkT}{q \cdot I} \approx \frac{40}{I\ (mA)} \quad \text{Ohm}$$

In this the AC impedance is inversely proportional to the applied current I. The voltage divider consists of a network of such diodes. The series path consists of diodes Gl 3 to Gl 10 and capacitors C 3, C 4, C 7, C 6 and C 8, together with resistor R 9 and inductance L 3. C 29 divides the input signal equally between the two halves of the series path at high frequencies. The parallel path consists of diodes Gl 11 to Gl 14 and Gl 16 to Gl 19 and capacitors C 9 and C 11. Each path of the divider consists of 4 diodes in series, to which a further 4 diodes in series are connected in parallel, but in the opposite direction. The resulting impedance of each path can therefore be represented as follows:

$$R_d \approx \frac{80}{I\ (mA)} \quad \text{Ohm}$$

It should be noted that all 8 diodes in each path are connected in series if they are regarded as a DC circuit. For this reason, all diodes present the small signal resistance. In contrast to this, regarded from the point of view of the signal flow, each path consists of 4 series diodes connected parallel to 4 series diodes with opposite polarity. The symmetry of this arrangement ensures that distortion products caused by signal currents, which are superimposed on the controlling DC signal, are negligible. The symmetry also reduces the distortions resulting from non-harmonic components. Furthermore, the distortion of harmonic components is reduced more by 4 series junctions than by one. At the same time, the signal voltage drop across each diode is reduced. The attenuation of the attenuator increases as the control voltage increases, as the direct current in the parallel diode path increases while the direct current in the series path decreases.

The control current for each path of the control element is generated by a symmetrical voltage, which is connected to the current-limiting resistors of each half of the diode arrangement. This results in a high degree of symmetry in each diode row and prevents variations of the control voltage from being propagated through the signal path, as this could endanger the possibility of the control loop. The control voltage is connected to an amplifier consisting of IC 1/3 and IC 1/4 which generates the symmetrical voltages. This supplies the parallel path of the control element and an inverter IC 1/1, which supplies the series path of the control element. In the parallel path of the control element, there is an inverting amplifier IC 1/3 which generates a voltage with precisely the same magnitude but the opposite polarity to that generated by the non-inverting IC 1/4. In this manner, voltages of the same magnitude but opposite polarities are connected via resistors R 15 and R 16 to the diode network. In the parallel path of the control element, it is necessary to increase the current considerably if a high attenuation is required. This is achieved with transistors T 3 and T 4, which increase the diode bias current in the parallel circuit in the case of a high control voltage.

The series path of the control element is supplied by IC 1/2 and the inverting IC 1/1. The inverting amplifier inverts the control voltage and generates a voltage offset with the aid of the network R 2, R 3, and Gl 21. The diode Gl 21 provides a temperature-dependent offset voltage

which compensates for the temperature coefficient of the control element. This type of compensation provides a stable ratio of the currents in the series and in parallel paths over the whole operating temperature range. The inverting amplifier IC 1/1 which supplies the series path has a DC gain of 2.3. This increases the sensitivity of the series path of the control element and simultaneously provides a constant loop gain over the whole attenuation range of the control element. In addition, the gain of the IC 1/1 is increased by R 35, C 27 and C 28 and high control loop frequencies. This gain increase compensates for the reduced sensitivity of the rectifier at low levels, to which reference will be made later.

R 39 and R 40 are current-limiting resistors which ensure that IC 1/1 and IC 1/4 are overdriven before IC 1/2 and IC 1/3. As the two latter ICs are inverting amplifiers fed by IC 1/1 and IC 1/4, they precisely simulate the form of the overdrive signal. This ensures that the control voltages for the series and parallel paths remain symmetrical even at high overdrive levels.

Resistor R 9 and coil L 3 represent the minimum impedance of the series path of the control element and thus determine its maximum attenuation. L 3 is a frequency-compensation element which compensates for the inductive component of the diodes in the parallel paths at high attenuations. The input impedance of the control element is approximately 110 Ω over the whole operating range. Resistor R 36 is used to increase this impedance to approximately 150 Ω.

As described in the previous sections, the control element generates an insertion loss for the applied signal which is approximately proportional to the connected control voltage. The output signal of the control element passes through the low-noise preamplifier, the second stage of the variable amplifier.

The low-noise preamplifier is a two-stage negative feedback amplifier consisting of T 1 and T 2. The gain of this wide-band amplifier is determined by R 22 and R 23 and is approximately 18 dB from 80 Hz to 25 MHz. The flat frequency response is achieved by shifting the phase of the negative feedback signal with the aid of a network consisting of C 15, C 16 and R 26. The components R 38 and C 24 provide gain correction at low frequencies. This is intended to compensate for the increased input load of the control element caused by R 6, R 7, C 2 and R 10, R 11 and C 5. R 30 determines the output impedance of the amplifier. When the amplifier is terminated, its gain is 12 dB.

As described above, the combination of control element and preamplifier guarantees a uniform voltage level over the frequency range 80 Hz to 25 MHz. The control element has a flat frequency response over its attenuation range of 7 to 18 dB. The output of the variable amplifier drives the final amplifier.

9.2.15.2 Output amplifier (2)

The output amplifier is a three-stage, wideband, negative feedback amplifier, whose output drives a complementary emitter follower stage which has two separate but identical outputs, each with an output impedance of 75 Ω. The gain of this amplifier is approximately 19 dB between 80 Hz and 25 MHz. The gain of the negative feedback amplifier consisting of T 1 to T 4 is determined by resistors R 12, R 13 and R 17 together with R 10. This type of negative feedback results in a parallel-series negative feedback amplifier. Additional frequency emphasis is achieved with components R 11, C 8, C 9, R 50 and C 44. This frequency emphasis network is intended primarily to compensate for the insertion loss of the output attenuator. At the same time, it results in a flat frequency response from the input to the output of the AGC amplifier, even if the control loop is open.

An additional gain of 5 dB is achieved by increasing the input impedance, this being switched with Rel 1. As described above, this gain increase is activated together with the 5 dB attenuator in the negative feedback attenuator. The AGC amplifier thus has an additional gain which is necessary at high output levels.

In the operating mode "normal time constant", a high-pass filter with a limit frequency of approximately 1.6 kHz is formed by the coupling capacitors C 39 and C 45. These oppose the input impedance of the negative feedback amplifier. If the operating mode "large time constant" is selected, the relay (Rel 2) for the loop speed is activated, and connects C 5 into the circuit. This shifts the lower limit frequency towards 80 Hz. At the same time, another relay contact closes a connection through L 9 and L 8 to the rectifier circuit. This increases the time constant of the rectifier in a manner which will become clear in the following description of the circuit.

The output of the negative feedback amplifier drives a complementary emitter follower stage T 5 and T 6, which has two separate outputs, each with an impedance of 75 Ω. The reflection coefficient of each output is improved by RC circuits consisting of R 47, C 35, C 31 and R 48, C 37, C 32. Output A drives the negative feedback loop via the loss-simulation circuit, while output B drives the output attenuator stage.

As described above, the output amplifier has a gain of approximately 19 dB. Two highly-decoupled outputs for the output attenuator and the negative feedback loop are provided. Together with the variable amplifier, the overall frequency response is flat, in the operating mode "large time constant" from 80 Hz to 25 MHz and in the operating mode "normal time constant" from 10 kHz to 25 MHz. Correction elements in the output amplifier provide emphasis in order to compensate for the insertion loss of the following output attenuator. Attention was paid to a flat frequency response from the input to the output over the whole operating frequency range.

9.2.15.3 Wideband attenuator (3)

The wideband attenuator is a precision attenuator whose switchable divider stages cover a range of 0 to 75 dB in 5 dB steps. It consists of 5 stages: three 20 dB attenuators, one 10 dB attenuator and one 5 dB attenuator. Each divider stage consists of one or two π-elements, which are constructed with highly-stable metal film resistors. Each attenuator is switched on or off by a miniature relay. Each attenuator contains elements for frequency compensation which are fitted during final testing in order to optimize the frequency response of each separate attenuator.

The insertion loss of the wideband attenuator results on the one hand from the contact resistance of the relays (which increases with the frequency) and on the other hand from the reactances which are distributed throughout this circuit. The increased resistance of the relay contacts is caused by the skin effect in the ferrous metals used in the relay. For this reason, the characteristic impedance at the inputs and outputs of the attenuators tend to increase with the frequency. This effect is virtually compensated by addition of RC circuits, which are inserted at the connection points of the attenuators. The purpose of these circuits is to reestablish the impedance of 75 Ω at the connecting points between the various attenuators. The correction elements which optimize the reflection factor of the attenuator consist of R 1 and C 1 at the input, of R 17 and C 5 in the third attenuator, of R 25 and R 7 in the fourth attenuator and of R 30 and C 9 in the fifth attenuator. The values of some of these RC circuits are modified during alignment. They ensure that a satisfactory reflection coefficient of the complete structure is maintained even if the relays are not activated.

An additional correction of the reflection coefficient is carried out at the outputs of the first 20 dB attenuator, of the 10 dB attenuator and of the 5 dB attenuator. These correction elements, consisting of C 17, C 18, C 20, C 21 and C 22, C 23, provide a satisfactory reflection coefficient at all combinations of the attenuators.

Additional correction circuits for the frequency response are used in the three 20 dB attenuators and in the 10 dB attenuator. These circuits consist of R 36, C 25 and C 14, R 37, C 26 and C 15, R 38, C 27 and C 16 and R 39, C 28 and C 19. These elements are adjusted during final alignment of the instrument in order to achieve an optimum frequency response for each attenuator.

As described above, the wideband attenuator can generate an attenuation of 0 to 75 dB in 5 dB steps over the whole frequency range. Extremely precise π- networks, supported by compensation elements for return and insertion loss, ensure very precise attenuation of the output signal on the AGC amplifier.

9.2.15.4 Relay control (8)

The relay control circuit converts the 5 V positive logic signals into 12 V switching signals in order to activate the relays in the AGC amplifier. In addition to the 5 relays in the wideband attenuator, this circuit controls the 5 dB negative feedback attenuator in the loss-simulation circuit and the 5 dB gain relay in the final amplifier. It also contains the control for the switch for the two time constants, which is also located in the final amplifier. As can be seen from the circuit diagram, two parallel drivers are used for the 5 dB switch in the negative feedback circuit, as the 5 V gain switch in the final amplifier is operated in parallel to this. In addition to voltage transformation of the logical signals for driving the relays, this circuit is also used to isolate the relays from the selection circuit, and thus to reduce the possibility of crosstalk between the relays via the selection circuit.

9.2.15.5 Loss-simulation circuit (4)

The most important function of the loss-simulation circuit, as its name indicates, is to generate an insertion loss with the frequency response which is practically identical to the insertion loss of the wideband attenuator and the external output circuit. The negative feedback loop therefore generates a signal which is slightly raised for the frequency response at the output of the wideband amplifier, in order to provide a signal with a flat frequency response at the output socket. In addition, the loss-simulation circuit contains one fixed and one switchable 5 dB attenuator. The frequency response of the insertion loss of the wideband attenuator consists of an extremely complex function. This almost completely compensates for the insertion loss of the relays. This insertion loss is due mainly to the skin effect in the ferrous materials used in the relays. This attenuation, which is equal to the square root of the frequency curve, is extremely difficult to simulate with discrete components. In the loss-simulation circuit, a coil consisting of a piece of iron wire similar to that used for the relay connections is used. This element has its maximum effect in the frequency range from approximately 100 kHz to approximately 10 MHz. The circuit provides space for pieces of wire which can be added during final alignment in order to compensate for the insertion loss of the wideband attenuator in this frequency range.

A further important factor which contributes to the insertion loss of the wideband attenuator is the three RC circuits in the 5 dB, 10 dB and first 20 dB attenuator. The attenuation caused by these circuits is compensated in the loss-simulation circuit with R 7, C 5 and C 6. R 12 and C 10 optimize the reflection factor at the input of the loss-simulation circuit. The RC circuit consisting of R 6, C 13, C 4 and the variable capacitors C 9 is used during alignment of the rectifier unit to provide a flat frequency response with the control loop closed.

A fixed 5 dB attenuator consisting of R 8, R 9, R 10 and R 11 separates the follow-up rectifier from the impedance of the equalizer.

The 5 dB negative feedback attenuator is a π-circuit and is constructed with precise metal film resistors. The RC circuit R 2, C 3 and the resonance circuit L 3 and C 11 provide adjustment facilities for the frequency response when the 5 dB attenuator is active.

The resonance circuits in the loss-simulation circuit have resonance frequencies which lie above 160 MHz. They are necessary to compensate for the internal impedances of the loss-simulation circuit.

As can be seen from the circuit diagram, many of the compensation elements are variable and can be adjusted during final inspection. This is necessary because the insertion loss of the wideband divider varies from one circuit to another. For this reason, the loss-simulation circuit is "married" in final inspection with a specific wide-band divider. This high flexibility in adjustment of the loss-simulation circuit and the extremely flat frequency response of the follow-up rectifier are responsible for the high performance of the AGC amplifier.

9.2.15.6 Follow-up rectifier (5)

The rectifier is the heart of the AGC amplifier. It consists, essentially, of two identical rectifiers. These process two signals, which come from the loss-simulation circuit and the reference divider. The filtered DC signals from the two rectifiers are fed to a differential amplifier which passes a highly-amplified difference signal to the control loop. A forward control circuit senses variations of the reference input level and passes a DC compensation voltage to the coupling capacitors at the input of the signal path and to the capacitor in the loop filter for large time constant. This ensures that the capacitors can reach their final charge rapidly. The forward control circuit drastically reduces the settling time of the AGC amplifiers after changes in the reference attenuator.

As can be seen in the circuit diagram, the follow-up rectifier consists of the double transistors T 1 and T 2, which are connected as diodes, and which are operated with a bias current of approximately 2 mA. The double transistors are selected for identical DC voltage temperature coefficients. Each half of the rectifier consists of two selected transistors with the same temperature coefficient. This achieves a high DC stability between the two rectifiers. Both signals, from the signal input and the reference input, which vary nominally between 0 and -4.9 dBm, are attenuated by approximately 14 dB before being connected to the diodes of the rectifier. The attenuators consist of R 7, R 6 and R 8 on the reference side and R 15, R 13, R 14 together with R 22 on the signal side. The frequency response for varying levels can be adjusted with C 13.

The output of the reference half of the reference rectifier is filtered with C 7. In the same manner, the output of the signal-half is filtered with C 16 and C 9. In the case of the operating mode "large time constant", C 8 is connected in order to increase the time constant by a factor of 11. Switching is carried out by the fast-slow relay in the final amplifier as described above. The filtered DC voltage signals of the two rectifier halves are connected via R 4 and R 3 to IC 1, a differential amplifier with a high gain. The gain of this differential amplifier, which is very high for DC voltages, drops by 6 dB per octave due to C 2 and C 3, and flattens out at 20 dB due to resistor R 2. This reversal frequency contributes primarily to the time constant in the control loop, as do C 9 and, in the operating mode "large time constant", C 9 plus C 8. The control voltage at the output of IC 1 is the highly-amplified differential voltage which exists between the two halves of the rectifier. This difference voltage is held at 0 V by the control loop when the circuit has settled.

A change in the reference input level results in a change of the DC voltage across C 7 and C 4. This voltage change causes, due to the loop gain of the control loop, a change in the level of the input signal. The resulting voltage across C 9 is equal to that across C 4. More important, however, is the fact that a DC voltage change corresponding to half the value across C 9 would be necessary in order to cause the same effect via the input coupling capacitors C 10, C 11 and C 12 at the signal input. The large time constant, together with these capacitors, would seriously increase the settling time of the control loop after changes in the reference level. In order to compensate for these voltage changes, the forward regulator consisting of IC 2/2 generates an input voltage change across resistor R 14 which is precisely equal to that necessary for the settled state. For this reason, no voltage change across the input coupling capacitors is necessary, and the settling time is not increased.

In the same manner, it will be necessary in the operating mode "large time constant" to match the voltage across C 8 to that across C 4. Due to the large time constant, this would drastically increase the settling time of the loop after changes of the reference level. In this case, the forward regulator generates a voltage step referred to the AC ground and parallel to C 8 via the fast-slow relay in the output amplifier. In this manner, the voltage across C 8 in the settled state does not change when the reference level changes. The settling behavior is improved. The rectifier is sensitive to noise from the supply voltage. In order to guarantee extremely low noise supply voltages, the positive and negative voltages are connected via active decoupling circuits. For the positive supply voltage, the decoupling circuit is located in the reference generator; for the negative voltage, it is in the control circuit. These active decoupling circuits supply the rectifier with $\pm$11.3 V.

As described above, the rectifier operates with selected pairs of rectifiers which process the reference voltage and the signal voltage. The resulting DC voltages are connected to a differential amplifier, and the amplified difference signal is connected to the control circuit.

9.2.15.7 Control circuit (9)

The control circuit generates a frequency-dependent correction of the control voltage in its magnitude and phase. It operates with the aid of the fast-slow control signal. The control circuit also includes the output blanking function, which uses a clamping circuit which generates the maximum possible control voltage and thus the maximum attenuation of the signal path. Furthermore, the circuit contains the active decoupling element for the negative supply voltage of -11.3 V for the rectifier.

The input signal of the control loop comes from the differential amplifier of the rectifier. In the operating mode "normal time constant" (fast), this signal passes via low-pass filter R 21 and C 9 to IC 1/1. In the fast operating mode, this amplifier has a DC gain of approximately 21 dB, determined by R 14 and R 16. As the frequency of the control voltage increases, the gain is increased with components R 15, C 12 and C 6 to its maximum value of approximately 33 dB. This network and the gain correction over the frequency provide the necessary phase correction in the transition of range. The output of IC 1/1 generates the control voltage via R 12 for the variable amplifier. R 12 is a plug-in resistor which permits the control loop to be opened for fault-finding purposes. A wave trap consisting of C 3, C 4 and L 1 is fitted at the control voltage output. This suppreses the 20 kHz from the reference generator. The diode, Gl 3, is also connected at the output to prevent the control voltage from reaching high negative values during settling.

The low-pass filter at the input, consisting of R 21 and C 9, has a limit frequency of approximately 9 kHz. This reduces the noise modulation on the high frequency signal which is generated in the control loop. The RC combination consisting of R 17, R 18 and C 5 provides a decoupled bias voltage at the input of IC 1/1 which suppresses unwanted overshoot during switching between the operating modes "large time constant" and "normal time constant".

In the operating mode "large time constant", the fast-slow control signal actuates two switches in IC 2. The first switch bypasses the negative feedback network of IC 1/1 and converts this into a linear voltage amplifier. The second switch connects capacitors C 7 and C 8 of the input circuit to ground. The resulting network at the input of IC 1/1 is now R 20, C 7, R 19 and C 8. This represents a second order low-pass filter which reduces the loop gain at very low frequencies when the large time constant is selected. In the operating mode "normal time constant", in which IC 2 is not active, C 8 is connected in series with C 7 and bypasses R 19, and therefore has a negligible effect. In both operating modes, the frequency-dependent gain, which is injected into the control loop by the control circuit, cooperates with other frequency-dependent components within the variable amplifier and the rectifier. These three circuits determine the overall negative feedback behavior and thus the settling behavior and loop stability of the AGC amplifier.

The second important function of the control circuit is the blanking function. If a logical 5 V signal is connected to the blanking input, it is connected via R 1, R 2 and the filter capacitor C 1 to the DC reference input of the rectifier. A voltage at the reference input rising positively causes the control voltage to rise rapidly and results in high attenuation of the high frequency. An active clamping circuit consisting of IC 1/2 monitors the control voltage and reduces the voltage connected to the reference input via R 4 and Gl 6, holding the control voltage at approximately 4.8 V. This results in maximum attenuation in the high frequency path. The blanking signal is connected at the same time to the reference attenuator, causing the reference signal at the input of the rectifier to be reduced. The combination of both operations results, in the control element, in an attenuation of at least 35 dB over the whole frequency band.

The control loop also has an input for an external reference voltage, which is connected via R 3 to the reference input of the rectifier. It should be noted, under these conditions, that the reference attenuator is set to maximum attenuation and the reference signal is determined exclusively by the externally-connected signal in the rectifier.

An auxiliary circuit in the control circuit is the active decoupling element T 2 for the rectifier. The -11.3 V generated here is strongly decoupled from the noise of the power supply unit and residual ripple from mains rectification.

As described above, the control circuit ensures that the negative feedback operates with a controlled frequency response and thus guarantees loop stability and best possible settling. In addition, the circuit contains the blanking function and limits the control voltage to a value between -0.7 and +4.8 V. This ensures that the control circuit always operates in its linear range.

9.2.15.8 Reference generator (6)

The reference generator generates a 20 kHz frequency with a stable level which is connected to the reference attenuator and then as the reference signal to the rectifier. The reference generator also contains the active decoupling of the positive supply voltage for the rectifier.

The reference generator is a Wien bridge oscillator consisting of IC 1 and the frequency-determining components R 1, C 1, R 2 and C 2. It is a well-known fact that a Wien bridge oscillator requires a voltage gain of precisely 3 in order to maintain its oscillation. The voltage gain of IC 1 is determined by R 5, R 3, R 4 together with the variable resistor represented by the field effect transistor T 1. The output amplitude of the reference generator is regulated by the control loop consisting of the peak rectifier IC 2/1, transistor T 2, filter capacitor C 7 and field-effect transistor T 1. IC 2/2 has a bias voltage in order to generate the maximum negative voltage of which the IC is capable at its output. This voltage is thus closely matched to the maximum negative output sweep of IC 2/1. This, in turn, generates a temperature-compensated emitter voltage for transistor T 2 and effectively eliminates changes due to temperature as the result of voltage changes at the emitter of T 2. T 2 is normally cut off and conducts only when the voltage at the inverting input of IC 2/1 exceeds -8.4 V. This occurs during extremely short current pulses through transistor T 2, which charge C 7 to a value between -1.8 and -3.2 V. This voltage is connected to the gate of T 1. The higher this negative voltage becomes, the higher is the resistance of T 1, and the higher R 3 and R 4 lie above ground. The variable resistance of T 1 maintains the voltage gain of the oscillator at precisely 3 and thus maintains the sinusoidal oscillation. The amplitude of the output signal is held at a nominal peak voltage of -8.4 V, depending on the precise value of the reference diode Gl 1. The output signal drives the reference attenuator via P 7 and R 8. The amplitude control loop has a long time constant determined by R 11 and C 7. Resistor R 16 damps settling oscillations which result when the supply voltage is connected to the circuit.

The decoupled +11.3 V supply voltage for the rectifier is generated by transistor T 3. This is a voltage with an extremely low noise value, free of noise from the voltage supply and from mains frequency components.

As described above, the reference generator provides a highly stable 20 kHz signal with a peak value which is determined by a very stable reference diode. This voltage is connected via a resistance network, which permits adjustment of the level over a very small range, into the reference attenuator. The output signal current is adjusted such that it delivers a maximum level of 0 dBm to the reference attenuator.

9.2.15.9 Reference attenuator (7)

The reference attenuator processes the signal from the reference generator. It provides precise attenuation in 0.1 dB steps between 0 dB and -7.9 dB. The output level of the reference attenuator is a signal in precise steps between 0 and -4.9 dBm, as 3 dB of the range are not used. The attenuator also has a blanking position which completely suppresses the output signal. In addition, small gain corrections of +0.03 dB (correction No. 1) and -0.04 dB (correction No. 2) are possible and can be superimposed on the setting of the attenuator.

The reference attenuator consists of three attenuator chains. Each of these can be switched by means of 8 x 1 semiconductor switches. Each attenuator chain is separated from the others by operational amplifiers acting as buffers. The input current from the reference generator is connected to amplifier IC 1/1, which presents a virtual ground for the reference generator. This means that the output voltge of IC 1/1 is determined by R 3 together with the output impedances of the reference generator. This voltage is approximately 0.55 V RMS. The output of IC 1/1 is connected to the first attenuator chain, whose output is selected by multiplexer IC 3. The selected output of IC 3 is connected through operational amplifier IC 1/2 to the second divider chain, whose output is selected with IC 4. The voltage selected with IC 4 is connected to operational amplifier IC 2/1, whose output signal passes to the third attenuator chain which is switched with IC 5. The output signal passes through the buffer amplifier IC 2/2 and resistor R 41 to the ouput of the reference attenuator. R 41 represents a 75 Ω source impedance for the reference input of the rectiifier. Transistor T 1 increases the current gain of IC 1/2 in order to guarantee an undistorted output signal.

Attenuation in the reference is carried out in three steps, as described above. The third divider chain, selected by IC 5, attenuator in 0.1 dB steps between 0 dB and 7 dB, corresponding to the BCD signals at pins a4, a2 and a3. The second attenuator chain, selected by IC 4, provides divider steps of 0 dB, 0.8 dB, 1 dB, 1.8 dB, 2 dB, 2.8 dB, 3 dB and 3.8 dB, corresponding to the logical signals at connection pins a7, a12 and a11. Finally, the first attenuator chain, selected by IC 3, provides large attenuator steps and the small correction values. This attenuator chain generates steps of +0.03 dB, -0.04 dB, -3.97 dB, -4.0 dB and -4.04 dB. Two other attenuator steps of approximately -20 dB or -24 dB can be connected into the circuit in accordance with the logical signals at pins a10, a9, a8.

The three attenuator chains together cover the normal attenuator range of 0 dB to 4.9 dB in 0.1 dB steps. Small attenuation corrections of -0.04 and +0.03 dB can be superimposed on this range. The reference divider also provides an additional attenuation of 20 dB. Normally, this step is used with the blanking function. Its accuracy is reduced and does not include the small correction factors.

Blanking of the reference generator is carried out via IC 5 with the blanking signal at pin a6. When the blanking signal is present, the output level of the reference generator is completely blocked. As described above, this, together with blanking of the control circuit, provides the maximum attenuation in the high frequency path.

As described above, the reference attenuator, which processes the signal from the reference generator, provides a precisely-controlled output level between 0 dBm and -4.9 dBm and passes this signal to the reference input of the rectifier. In addition, this signal can be attenuated via a further 20 dB or completely blocked by means of the blanking input.

9.2.15.10 Negative feedback loop

The negative feedback loop is an extremely complex, non-linear circuit whose characteristics can be described only approximately over a small working range.

Two special non-linear elements are used in the control loop. The first is the rectifier, which operates as an RMS detector. It has a high sensitivity as a function of the input level. At an output level of 0 dBm, the rectifier has a sensitivity of approximately 250 mV for a level change of 0.01 dB. At an output level of -4.9 dBm, the sensitivity is approximately only 80 mV for a level change of 0.01 dB. The rectifier sensitivity varies by approximately 10 dB over the normal working range of the rectifier. This varying sensitivity explains the characteristic curve of the control loop.

The second important non-linear element is the sensitivity of the control element as a function of the required attenuation. If it is remembered that the impedance of the control element diodes varies inversely with the injected current, then it is apparent that the attenuation sensitivity of the control element is directly dependent on the working point. Either the series or the parallel path reduces its sensitivity as the current increases, and the sensitivity increases when the current drops.

In the control element, these two effects virtually counteract each other. Whereas the sensitivity in the parallel path drops, the control current rises. At the same time, the sensitivity in the series path rises and the current drops. Over the working range of the control element, the sensitivity thus remains sufficiently constant.

The limit frequency of the control element, regarded from the control loop point of view, is determined by the parallel path consisting of R 15, R 16, C 9, C 11 and the instantaneous impedance of the voltage divider of the parallel diodes. At an output level of 0 dBm, the nominal current in the series and parallel paths is approximately 0.5 mA. Under these circumstances, the limit frequency of the parallel path is approximately 29 Hz. This is much lower than that of the series path, and is thus dominant in the frequency behavior of the control element with the control loop open. It is important to note that the limit frequency varies as a function of the control voltage. However, this behavior is accompanied by a change in the sensitivity such that the sensitivity of the parallel path drops as the limit frequency rises. This means that the change in sensitivity is unimportant for frequencies above the limit frequency of the control element.

Under these circumstances, the sensitivity of the control element can, as a first approximation, be regarded as linear with a single, simple pole at approximately 29 Hz. For the following sections, it should be remembered that this is an approximation and that the actual circumstances are to a high degree non-linear and deviate considerably from this ideal representation. Nevertheless, this is sufficiently accurate in order to determine the settling behavior and the stability of the control loop.

As mentioned above, the rectifier's sensitivity varies by 10 dB over its operating range. In order to understand the function, it is necessary to know that the sensitivity drops slowly as the output level of the reference attenuator decreases and, as a result, requires an increase in the attenuation of the control element. This increase, as mentioned above, is determined primarily by the behavior of the series path of the voltage divider. In order to compensate for the reduction in the sensitivity of the rectifier, the gain of the drive circuit in the series path is increased. This is achieved by components R 35, C 27, C 28.

This combination causes a gain increase, starting at approximately 10 Hz and ending at approximately 30 Hz, for the series path of the control element. This gain increase compensates for the reduced sensitivity of the rectifier at low levels.

The loop gain is dimensioned such that the stability is guaranteed over the whole control range and that the settling behavior has only a slight tendency to overshoot.

With the fast time constant, the loop gain passes through 0 dB at 400 Hz. In the slow mode (large time constant), the loop gain passes through 0 dB at 17 Hz.

9.2.16 OUTPUT SECTION (16)

Circuit diagram 870-7516

9.2.16.1 Overall function of the output section

The task of the output section is to switch the 75 Ω output of the AGC amplifier through to one of the three outputs of the complete unit. Due to the relay logic used, it is possible to obtain a signal only at one output, and not at several outputs simultaneously.

The three possible outputs are:

1) Output UNBAL, unbalanced, 80 Hz ... 25 MHz, Z_{out} = 75 Ω

2) Output BAL. I, balanced, 60 kHz ... 14 MHz, Z_{out} = 124/150 Ω

3) Output BAL. II, balanced, 80 Hz ... 620 kHz, Z_{out} = 0/150/600 Ω.
(see block diagram of output section on next page)

For the UNBAL output, the signal of the AGC amplifier is switched directly through the circuit without frequency response correction, because the frequency response of the connecting cable, of the switching relay, and of the other connecting elements is simulated in the control loop of the AGC amplifier. This ensures that these losses are compensated in the control element of the AGC amplifier as far as the output. The signal from the AGC amplifier is connected to the output BAL. I via a balancing transformer. This provides balancing and conversion to Z_{out} = 124 Ω or Z_{out} = 150 Ω.

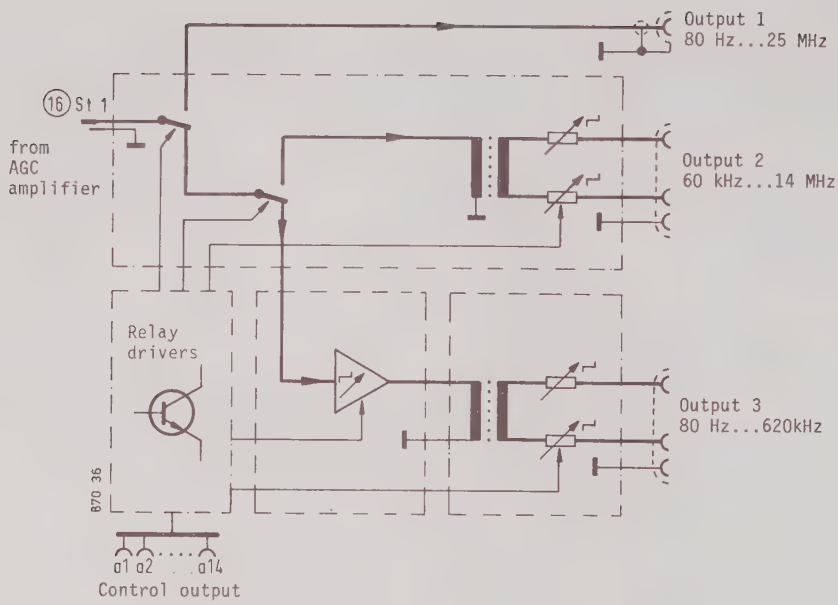


Figure 9-7 Block diagram of output section

The signal path for the output BAL. II contains, in addition to a balancing transformer, an isolating amplifier which provides an output impedance Z_{out} = 0 and an additional increased level of "10 dB". The input impedance of the isolating amplifier is 1 kΩ.

9.2.16.2 Board "Output 2"

(See circuit diagram)

The board "Output 2" contains, in addition to the balancing transformer for output BAL. I, the switching of the input signal to the various outputs (REL. 5 and REL. 4).

As the contacts of these two relays are connected in series, only one output can be activated even if the relays are driven incorrectly.

This board also implements the direct connection to output UNBAL. In order to keep the transfer characteristics as constant as possible, the leads on this board are designed as 75 Ω strip conductors.

The transformer $Ü_1$ should, in order to avoid level losses, act as a transformer for power levels, i.e. it should tranform the 75 Ω source impedance of the AGC amplifier into the required value of 124 Ω or 150 Ω. As, however, the transformer can have only integral numbers of turns in its windings, the required theoretical conversion ratio cannot be achieved precisely. In addition, transformation into two different impedances is necessary. In order to achieve this, the integral conversion ratio which is as close as possible to, but still below, the required value of 124 Ω was selected. The resulting impedance, which is too low, is supplemented to 124 Ω by resistors R2 and R4 or to 150 Ω by R3 and R5.

The resulting slight level loss is corrected by the computer in that it increases the amplifier output voltage accordingly.

The capacitors C_2 and C_4 or C_3 and C_5 across the supplementary resistors are intended to slightly increase the frequency response at the upper end of the frequency band. In addition,

the resonant increase of the series-tuned circuit, which results from the leakage inductance of the transformer and the existing parallel capacitances, is utilized to increase the frequency response:

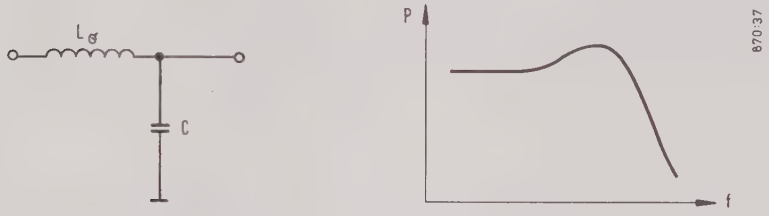


Figure 9-8 Boosted frequency response at higher frequencies

The capacitor C1 and the main inductance provide a frequency response increase for low frequencies, which uses the same principle as above:

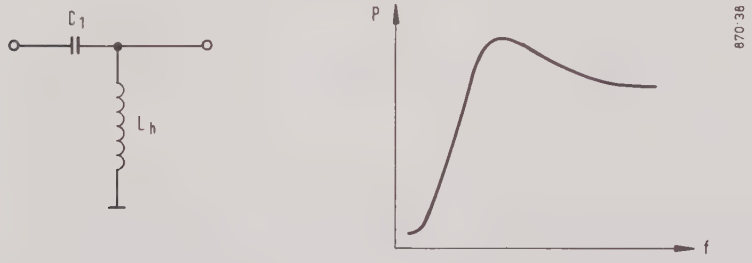


Figure 9-9 Boosted frequency response at lower frequencies

The resistance of the transformer, together with the source impedance of the amplifier, forms a voltage divider whose division ratio will vary according to the true values of the components. This variation is compensated for setting the division ratio with R1 and P1 to a constant value. The resulting transformer loss, which is always constant, is taken into account and corrected together with the other losses of the circuit in the computer program for level setting.

9.2.16.3 Output amplifier board

The output amplifier consists mainly of three amplifier stages, a negative feedback loop, and an offset regulation circuit:

(See block diagram of the amplifier on the following page)

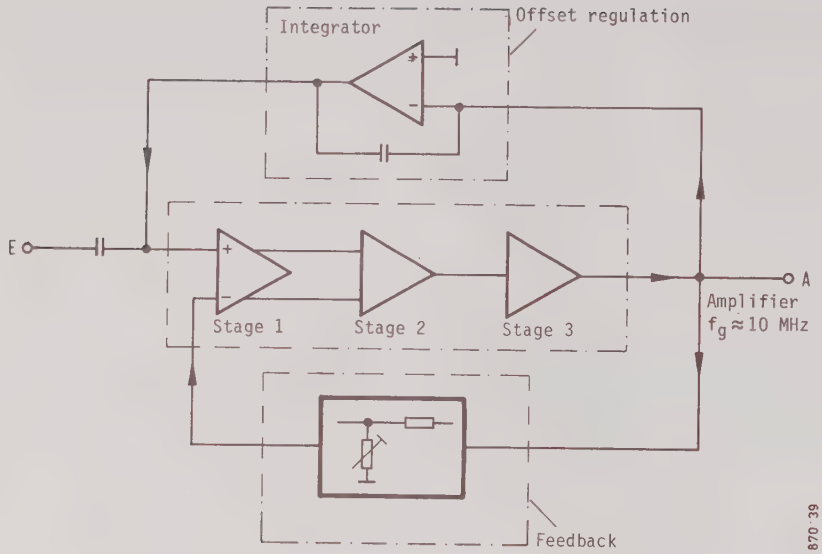


Figure 9-10 Block diagram of output amplifier

The first stage with T_1, T_2, and T_3 is a differential amplifier with a gain of 20 dB. The following current push-pull circuit with T_5 and T_6 provides a further voltage gain of 40 dB. The last stage consists of IC 1. This contains an emitter-coupled complementary push-pull output stage in order to provide the necessary load current (current gain approximately 30 dB). The voltage gain of this circuit is approximately 0 dB. Resistors R_{34}, R_{36} limit the current in the case of a short circuit; for thermal reasons, the amplifier output can withstand the short circuit for not more than approximately 1 minute.

A passive negative feedback path over all three stages of the amplifier is used for gain adjustment and frequency response compensation. The resistors, R_{40}, R_{41} and the trimmer P_2 are used for voltage adjustment for "0 dB" gain. Resistors R_{40}, R_{42}, R_{43} and trimmer P_3 are used for setting the "10 dB" level.
The actual gain is, however, approximately 0.5 dB or 10.5 dB, respectively.
The frequency response at the upper end of the frequency band is corrected with C 32 and L 1 and C 36/ C 37.
In order to prevent biasing of the following transformer 0_2 by the direct current, IC 2 regulates the DC voltage offset of the output amplifier to 0 V.

9.2.16.4 "Output 3" board

The transformer on the board "Output 3" balances the output of the "Z_{out}= 0" amplifier and is matched with the appropriate resistors R 141, R 142, R 143, R 144 to the impedances Z_{out} = 150 Ω/600 Ω. The capacitors C 41, C 43, C 44, C 45 are used for frequency response correction at the upper end of the frequency band. C 41 corrects the frequency response in the case Z_{out} = 0, Z_L = 150 Ω.
C_{46} provides additional balancing of the transformer, a further increase of the C value for alignment purposes being provided on the board (C 47).

9.2.16.5 Relay driver board

The relay driver board receives the control signals and the supply voltages via a 14 pin ribbon cable from the CPU motherboard.
As the power of the control signals is too low, they must be amplified. This is done with one transistor per control signal. The only exception to this is relay 6, which can be activated only if relay 1 is active. Diode G1 16 increases the common emitter potential in order to ensure that the undriven transistors are cut off.

9.2.17 CARRIER SWITCH (17)

Circuit diagram 870-7517

This board contains a changeover switch for selection of two different carrier signals. In order to achieve a good off isolation, three relays are used and all lines which are not being used are connected to ground.

9.2.18 IEC BUS BOARD

Figure 9-11 shows the simplified block diagram of the Interface Bus <IEC 625> board.

The interface to the <IEC 625> Bus with the necessary driver and receiver circuits is shown on the right.
The connections to the input/output Bus of the internal microprocessor are shown on the left. For the microprocessor, the <IEC 625> interface is nothing more than a collection of entry gate and output ports, via which data are exchanged between the <IEC 625> Bus and the measuring set. The exchange of data between the <IEC 625> Bus and the measuring set is controlled by the IEC Bus program. The PROMs in which this program is stored are not located on the <IEC 625> interface board, but in the measuring set itself.

The actual interface logic is contained in one IC: the IEC Bus interface module MC 68 488 from Motorola. This interface logic handles most of the interface tasks independently, i.e. without using the internal microprocessor; for example, it independently carries out the <IEC 625> Bus handshake cycle and decodes all messages which are transferred on the <IEC 625> Bus.
The interface states resulting from these messages are written into the appropriate entry gates.

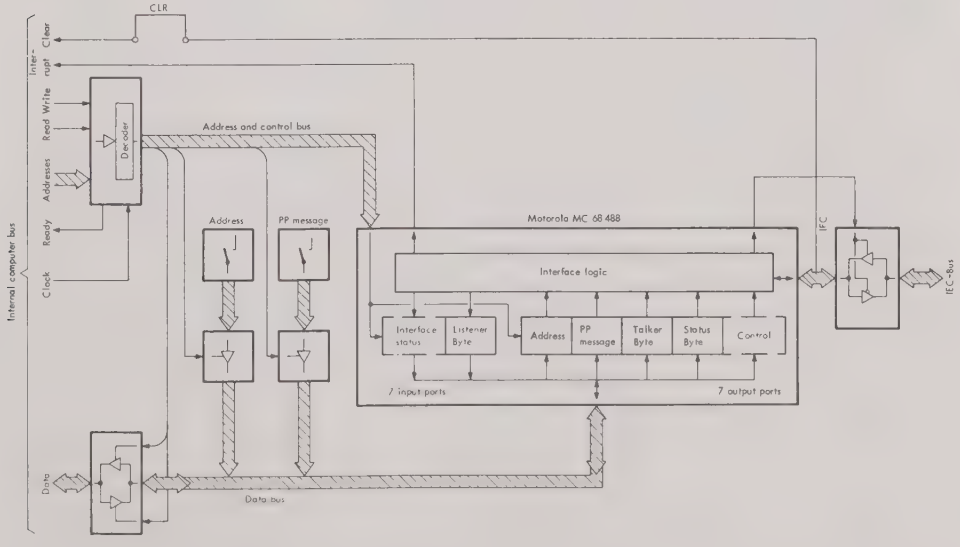


Figure 9-11 Block diagram of <IEC 625> Interface

A further entry gate acts as a transfer register for listener bytes. Listener bytes are data which are transferred from the <IEC 625> Bus to the device as long as the device is addressed as the listener, for example, when setting parameters are transferred to the device.

In addition to the entry gates, the module contains output gates. These are used

- for reception of control commands with which the microprocessor can control the behaviour of the Interface logic (for example, it can, amongst other things, stop the handshake cycle or transmit a service request SRQ via the <IEC 625> Bus).
- as a transfer register for bytes which are to be transferred from the device to the <IEC 625> Bus, for example, talker bytes and status byte.
  Talker bytes are data which are transferred from the device to the <IEC 625> Bus as long as the device is operating as the talker, for example when the result of measurement is transferred.
  The status byte is the response of the device to a serial poll and contains the current device status.

The device address can be set up on the address switch.

With the "PP switch", the data line of the IEC Bus on which the device transits its status bit PQS when the controller carries out a status request by means of parallel poll can be determined.

Cooperation between the device and <IEC 625> Interface

When the <IEC 625> Bus has reached a state in which operation by the internal microprocessor is necessary, the <IEC 625> Interface sends an interrupt to the device. As a result of this interrupt the microprocessor executes the IEC Bus program (see Figure 9-12). This is always the case:

- when the device is to be switched from local control to remote control or from remote control to local control.
- when a listener byte was transferred via the <IEC 625> Bus. The Interface logic has then placed this byte in the transfer register for listener bytes and stopped the handshake cycle. The handshake cycle remains interrupted until the microprocessor has read this byte (when NDAC becomes high). After processing and storage of the listener byte, NRFD = high is transmitted.
- when the device must provide a new talker byte. The handshake cycle is restarted (DAV = low) when the new talker byte has been written into the appropriate output gate.
- when the device is to be initiated for a new measurement via the <IEC 625> Bus command "device trigger (GET)". The Interface logic has now stopped the handshake cycle. This remains interrupted until the microprocessor has started the measurement and then again enables the handshake cycle (NDAC = high and NRFD = high).
- If the device is to be placed in a defined initial status by means of the <IEC 625> Bus command "Device Clear (DCL or SDC)". Again, the Interface logic stops the handshake cycle and it remains interrupted until the microprocessor has set the device to the initial status and then enables the handshake cycle again (NDAC = high and NRFD = high).

If the strap CLR is fitted on the <IEC 625> Interface board, the <IEC 625> Bus signal IFC (Interface clear) causes the device to be initialized. This permits the device to be initialized by the <IEC 625> Bus in all cases, even if it has locked itself up (this is important for devices in unmanned stations, where an external fault may cause a lock-up which cannot be cleared by switching the mains voltage off and on again).

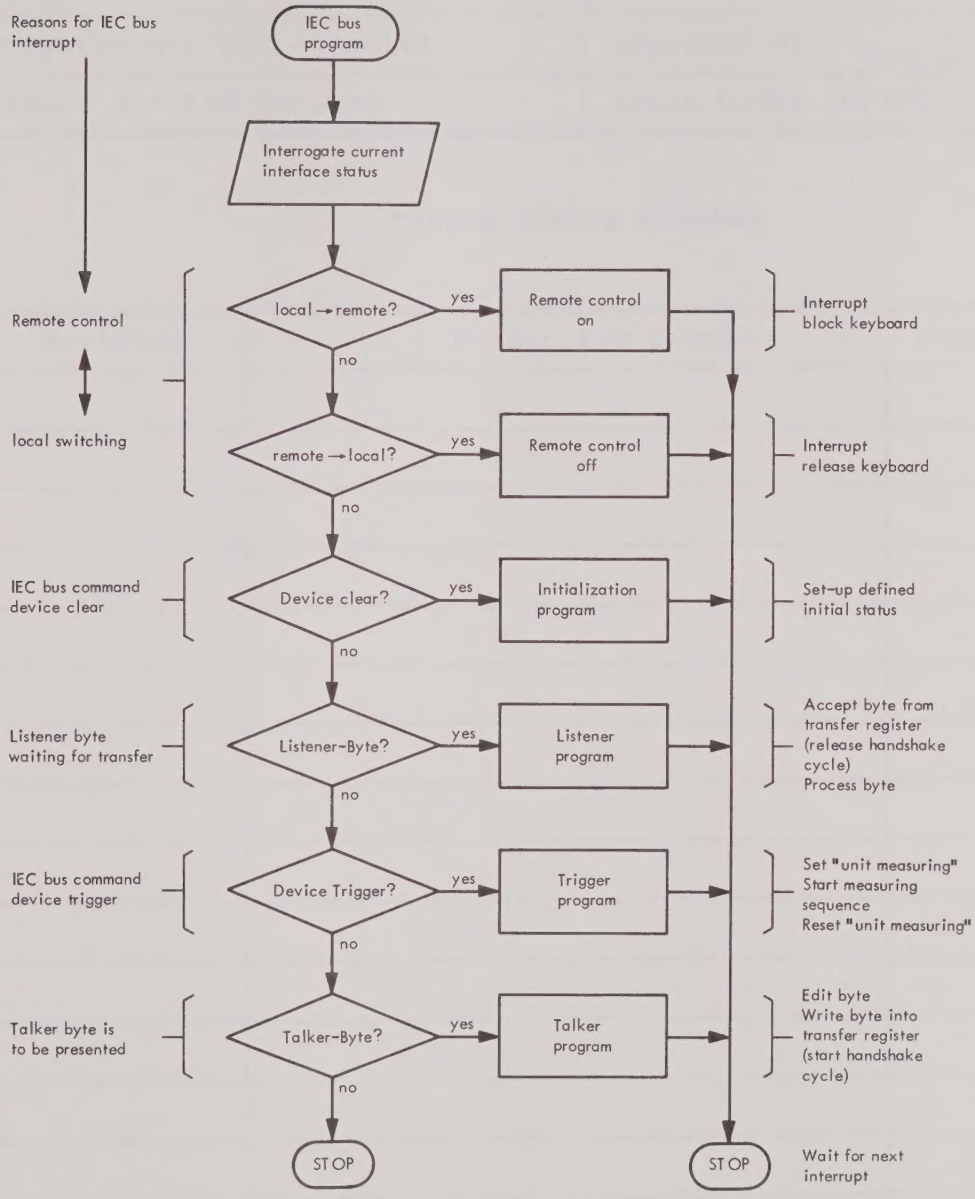


Figure 9-12 Structure of the Interface Bus Program

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